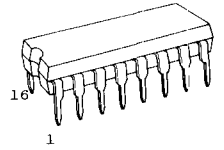
TC74HC298P QUAD 2-CHANNEL MULTIPLEXER WITH OUTPUT REGISTER

GENERAL DESCRIPTION

The TC74HC298 is a high speed CMOS 2-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It contains a 4 bit 2-channel multiplexer and a 4-bit output register. When the word-select input (W.S.) is held low, word 1 (A1, B1, C1, D1) input data is selected and is applied to the registers. On the other hand W.S. is held high, word 2 (A2, B2, C2, D2) input data will be applied to the registers. This selected data is transfered to the output terminals (Q_A, Q_B, Q_C, Q_D) on the negative-going transition of the clock pulse ($\overline{CLOCK}$).
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{PLH}\fallingdotseq t_{PHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS298



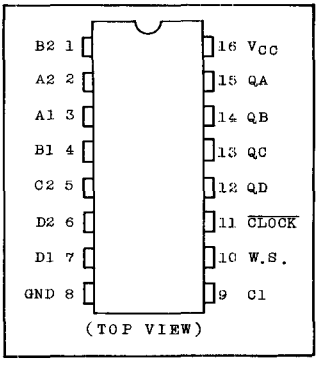
DIP(5-22E)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



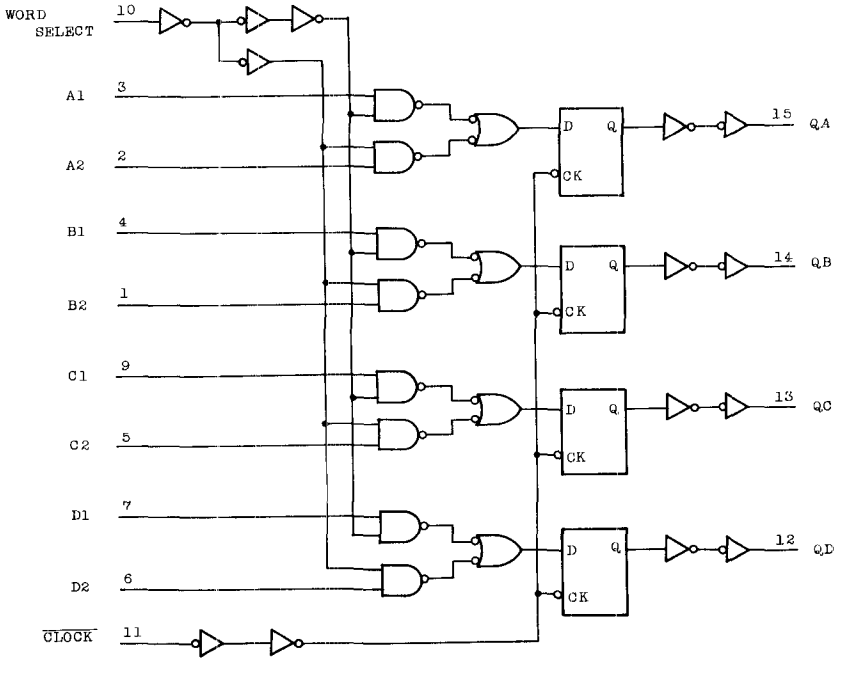
(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	$\overline{CLOCK}$	QA	QB	QC	QD
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	↓	QA0	QB0	QC0	QD0

X : DON'T CARE(INCLUDING TRANSITION)
a1,a2, ETC. : THE LEVEL OF STEADY-STATE INPUT AT A1,A2,ETC.
QA0,QB0,ETC. : THE LEVEL OF QA,QB,ETC. ENTERED ON THE MOST RECENT NEGATIVE TRANSITION OF THE CLOCK INPUT.

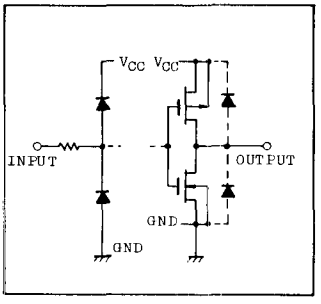
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.32	-	0.37	
			I_{OL}=5.2mA	6.0	-	0.18	0.32	-	0.37	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	90	ns
			4.5	-	8	15	-	18	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	70	150	-	180	
			4.5	-	19	30	-	36	
($\overline{CLOCK}$ - Q)	t_{pHL}		6.0	-	17	26	-	31	
Minimum Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	90	
			4.5	-	7	15	-	18	
($\overline{CLOCK}$)	$t_{w(L)}$		6.0	-	6	13	-	16	
Minimum Set-up Time	t_s		2.0	-	20	75	-	90	
			4.5	-	4	15	-	18	
(A, B, C, D)			6.0	-	3	13	-	16	
Minimum Set-up Time	t_s		2.0	-	35	75	-	90	
			4.5	-	8	15	-	18	
(W.S.)			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
(A, B, C, D, W.S.)			6.0	-	-	4	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	47	-	-	-	

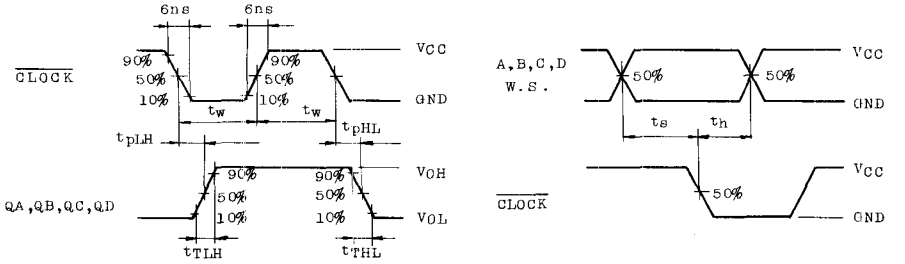
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per bit)}$$

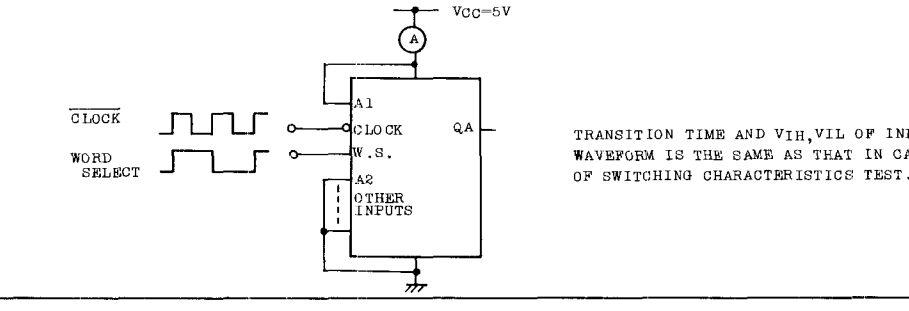
And the C_{PD} for the operating n-bit can be obtained by the following equation.

$$C_{PD} = 32 + n \cdot 15$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

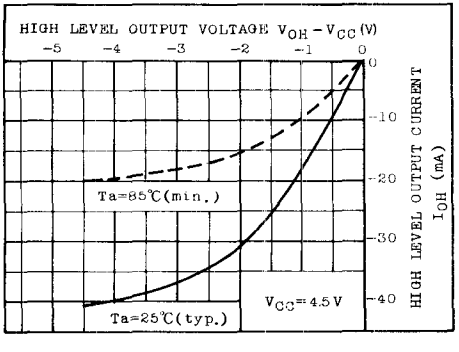


$I_{CC(opr.)}$ TEST CIRCUIT

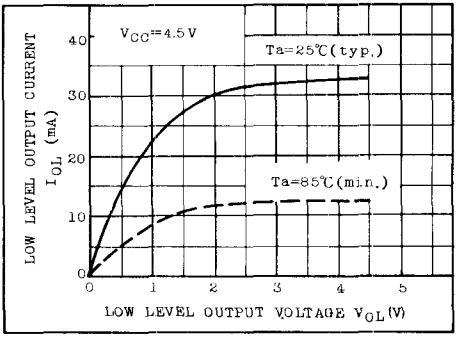


TRANSITION TIME AND VIH, VIL OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

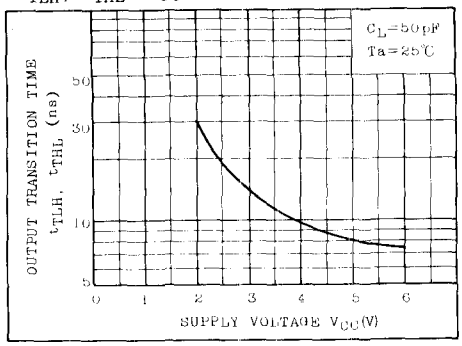
I_{OH} CHARACTERISTICS



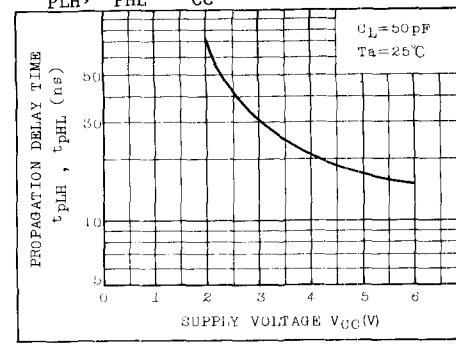
I_{OL} CHARACTERISTICS



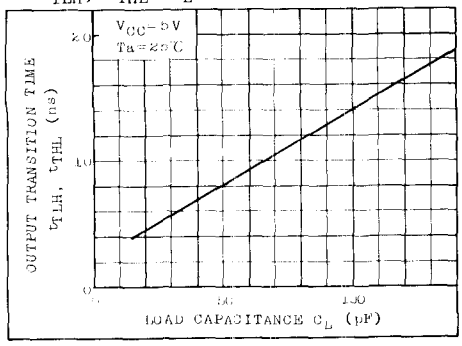
t_{TLH}, t_{THL} - V_{CC} CHARACTERISTICS (TYP.)



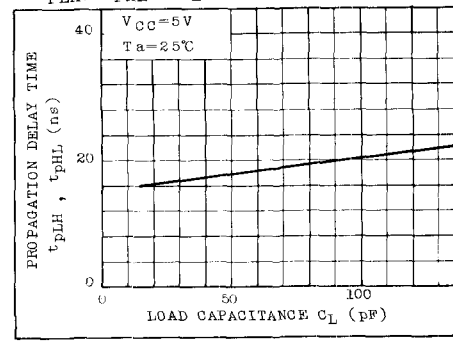
t_{PLH}, t_{PHL} - V_{CC} CHARACTERISTICS (TYP.)



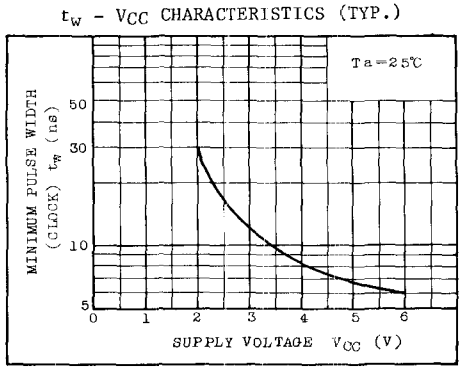
t_{TLH}, t_{THL} - C_L CHARACTERISTICS (TYP.)



t_{PLH}, t_{PHL} - C_L CHARACTERISTICS (TYP.)



t_W - V_{CC} CHARACTERISTICS (TYP.)



t_S - V_{CC} CHARACTERISTICS (TYP.)