

MITSUBISHI HIGH SPEED CMOS
M74HC133P/FP/DP

13-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74HC133 is a semiconductor integrated circuit consisting of a 13-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High-speed: 20ns typ. ($C_L=15\text{pF}$, $V_{CC}=5\text{V}$)
- Low power dissipation: $5\mu\text{W}/\text{package}$, max ($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, quiescent state)
- High noise margin: 30% of V_{CC} , min ($V_{CC}=4.5\text{V}$, 6V)
- Capable of driving 10 74LSTTL loads
- Wide operating voltage range: $V_{CC}=2\sim 6\text{V}$
- Wide operating temperature range: $T_a=-40\sim +85^\circ\text{C}$

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

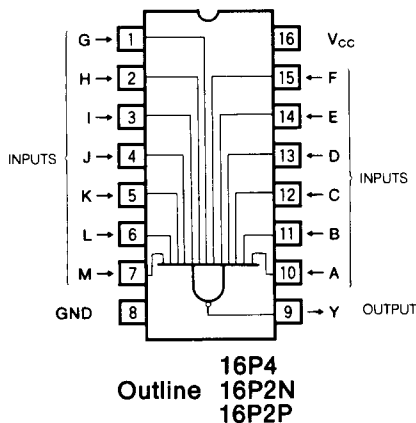
FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC133 to maintain the low power dissipation and high noise margin of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS133.

Buffered output Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When inputs A through M are all high, the output Y will become low and when at least one of A through M is low, the output Y will become high.

PIN CONFIGURATION (TOP VIEW)

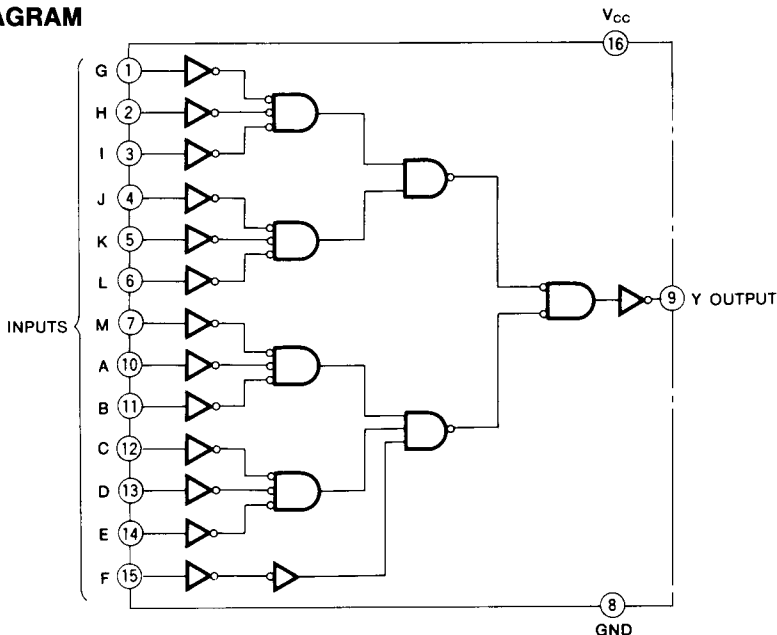


FUNCTION TABLE

Inputs		Output
A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

$N = B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M$

LOGIC DIAGRAM



13-INPUT POSITIVE NAND GATE

ABSOLUTE MAXIMUM RATINGS (T_a = -40~+85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{CC} +0.5	V
V _O	Output voltage		-0.5~V _{CC} +0.5	V
I _{IK}	Input protection diode current	V _I < 0V	-20	mA
		V _I > V _{CC}	20	
I _{OK}	Output parasitic diode current	V _O < 0V	-20	mA
		V _O > V _{CC}	20	
I _O	Output current per output pin		±25	mA
I _{CC}	Supply/GND current	V _{CC} , GND	±50	mA
P _d	Power dissipation	(Note 1)	500	mW
T _{stg}	Storage temperature range		-65~+150	°C

Note 1 : M74HC133FP, T_a = -40~+70°C and T_a = 70~85°C are derated at -6mW/°C.
M74HC133DP, T_a = -40~+50°C and T_a = 50~85°C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS (T_a = -40~+85°C)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	2		6	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
T _{opr}	Operating temperature range	-40		+85	°C
t _r , t _f	Input risetime, falltime	V _{CC} = 2.0V	0	1000	ns
		V _{CC} = 4.5V	0	500	
		V _{CC} = 6.0V	0	400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits					Unit	
			V _{CC} (V)	25°C			-40~+85°C		
				Min	Typ	Max	Min		Max
V _{IH}	High-level input voltage	V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2	V	
V _{IL}	Low-level input voltage	V _O = V _{CC} - 0.1V I _O = 20μA	2.0 4.5 6.0		0.5 1.35 1.8		0.5 1.35 1.8	V	
V _{OH}	High-level output voltage	V _I = V _{IH} , V _{IL}	I _{OH} = -20μA	2.0	1.9		1.9	V	
			I _{OH} = -20μA	4.5	4.4		4.4		
			I _{OH} = -20μA	6.0	5.9		5.9		
			I _{OH} = -4.0mA	4.5	4.18		4.13		
			I _{OH} = -5.2mA	6.0	5.68		5.63		
V _{OL}	Low-level output voltage	V _I = V _{IH}	I _{OL} = 20μA	2.0		0.1	0.1	V	
			I _{OL} = 20μA	4.5		0.1	0.1		
			I _{OL} = 20μA	6.0		0.1	0.1		
			I _{OL} = 4.0mA	4.5		0.26	0.33		
			I _{OL} = 5.2mA	6.0		0.26	0.33		
I _{IH}	High-level input current	V _I = 6V	6.0		0.1		1.0	μA	
I _{IL}	Low-level input current	V _I = 0V	6.0		-0.1		-1.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} , GND, I _O = 0μA	6.0		1.0		10.0	μA	

13-INPUT POSITIVE NAND GATE

SWITCHING CHARACTERISTICS ($V_{CC} = 5V, T_a = 25^\circ C$)

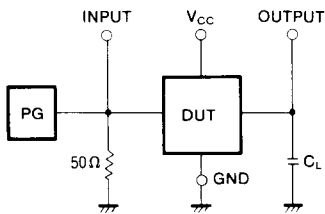
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	$C_L = 15pF$ (Note 3)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (A, B, C, D, E, F, G, H, I, J, K, L or M - Y)				30	ns

SWITCHING CHARACTERISTICS ($V_{CC} = 2\sim 6V, T_a = -40\sim +85^\circ C$)

Symbol	Parameter	Test conditions	Limits						Unit
			$V_{CC}(V)$	25°C			-40~+85°C		
				Min	Typ	Max	Min	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	$C_L = 50pF$ (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}	output transition time		2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level	2.0			160		190	ns	
		4.5			35		42		
		6.0			30		36		
t_{PHL}	output propagation time (A, B, C, D, E, F, G, H, I, J, K, L or M - Y)	2.0			160		190	ns	
		4.5			35		42		
		6.0			30		36		
C_I	Input capacitance				10		10	pF	
C_{PD}	Power dissipation capacitance (Note 2)			32				pF	

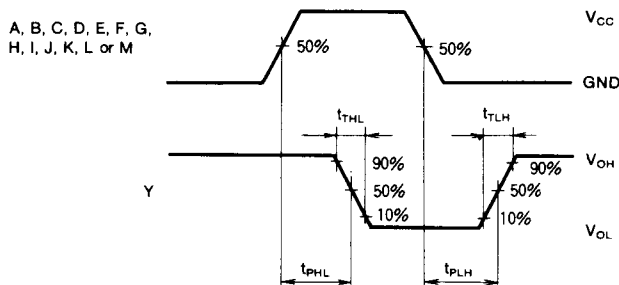
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipated during operation under no-load conditions is calculated using the following formula:
 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns, t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES

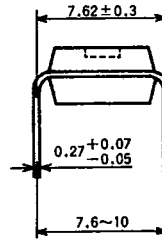
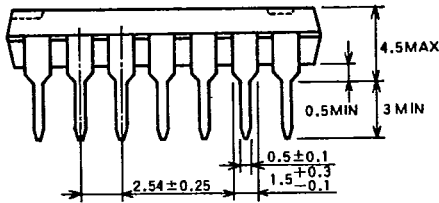
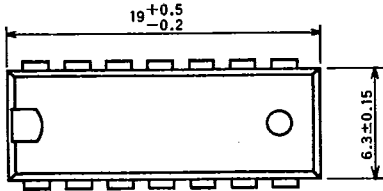
6249827 MITSUBISHI (DGTL LOGIC)

91D 12849

D T-90-20

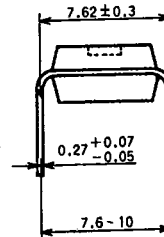
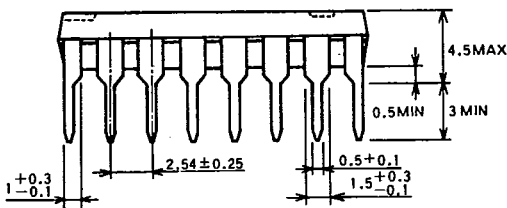
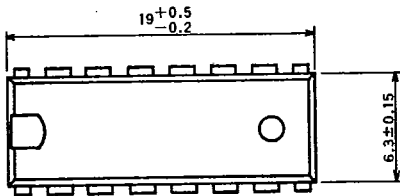
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

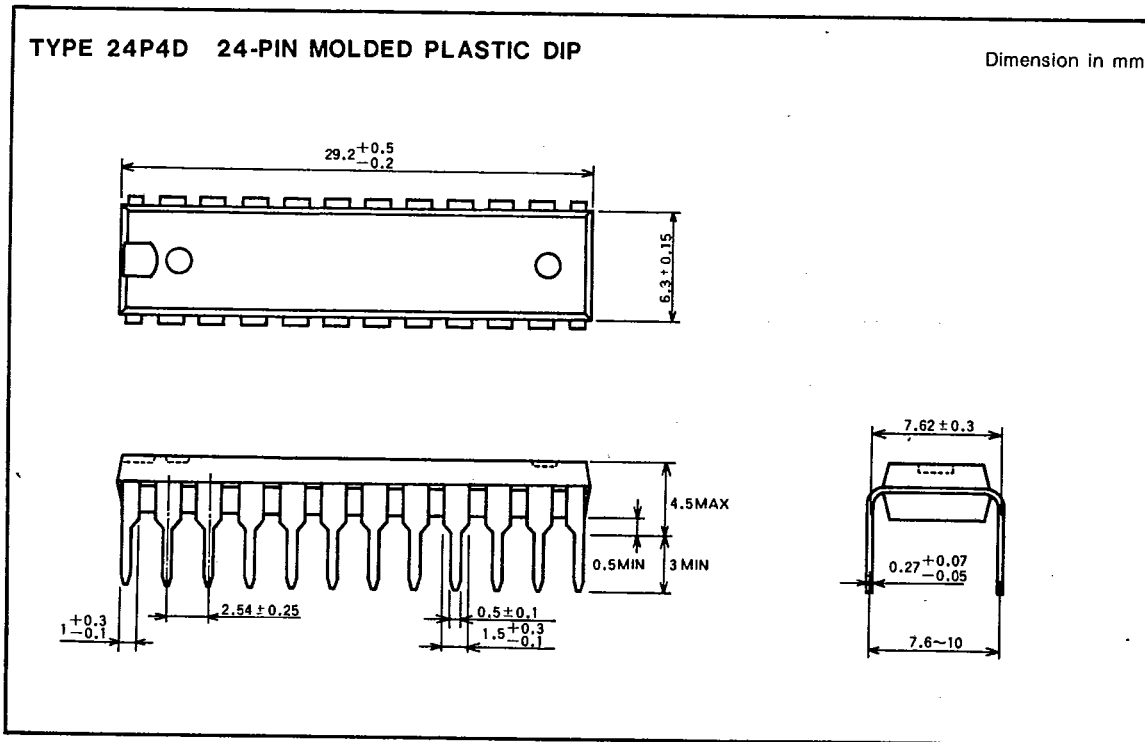
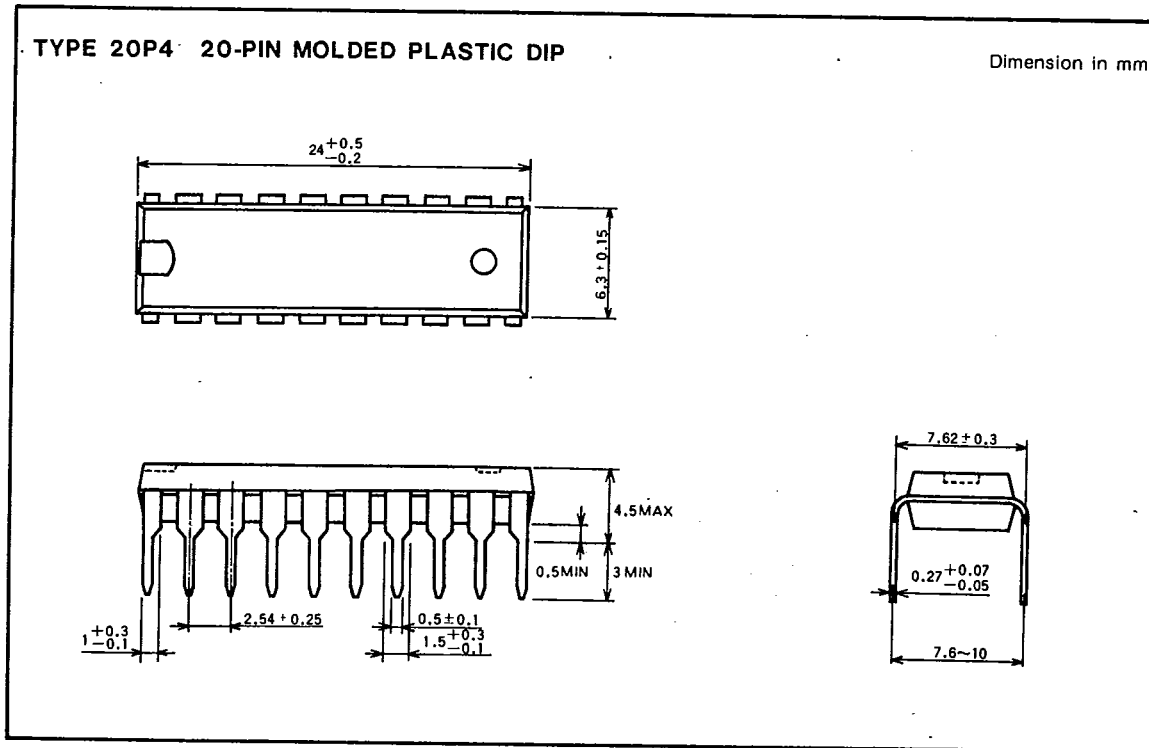
Dimension in mm



MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12850 D.T-90-20



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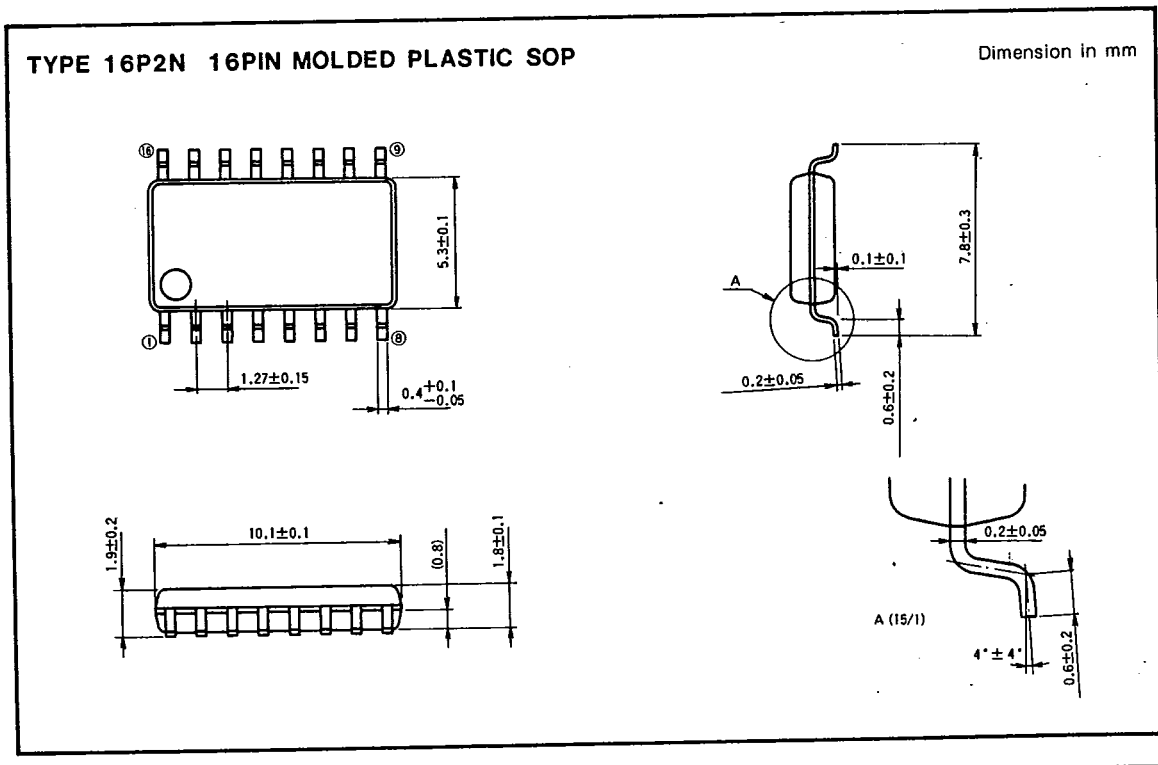
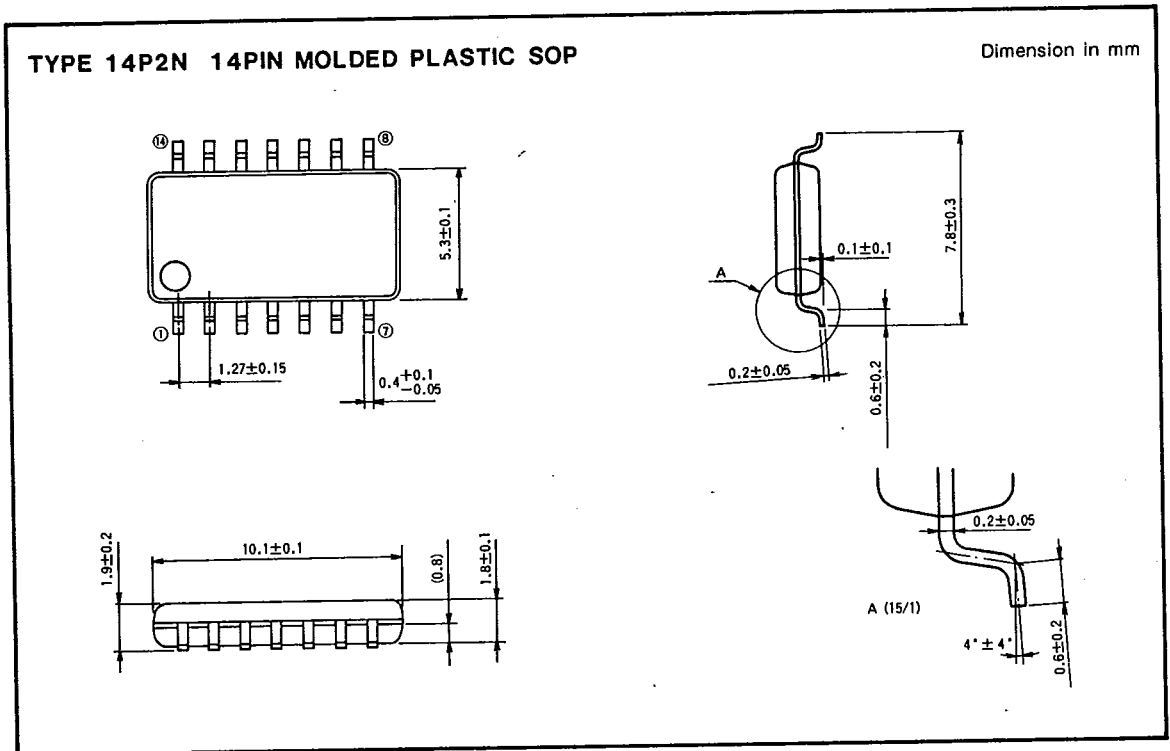


MITSUBISHI ELECTRIC CO. TOKYO, JAPAN

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PACKAGE OUTLINES

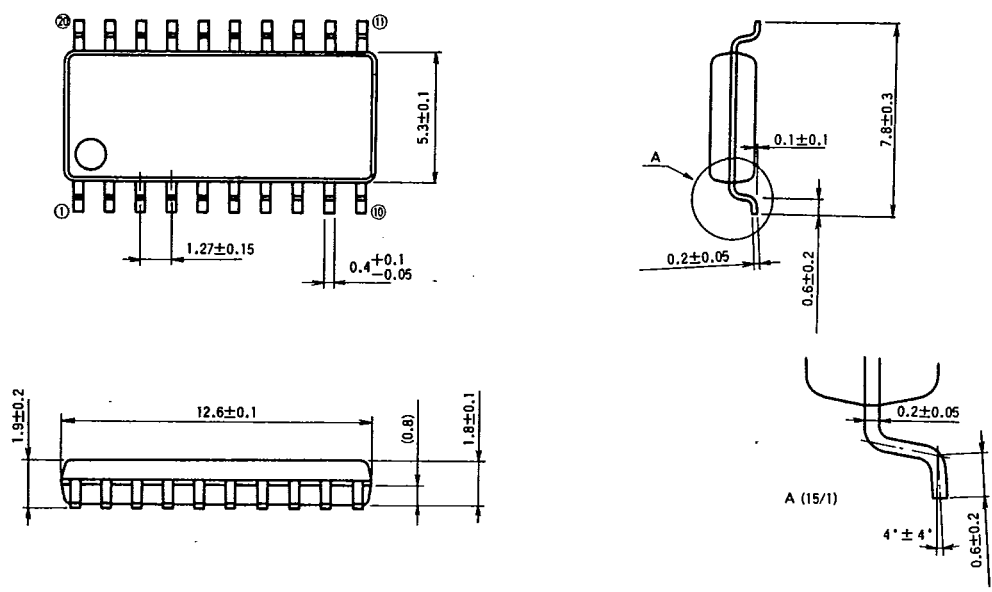
6249827 MITSUBISHI (DGTL LOGIC)

91D 12851 D T-90.20



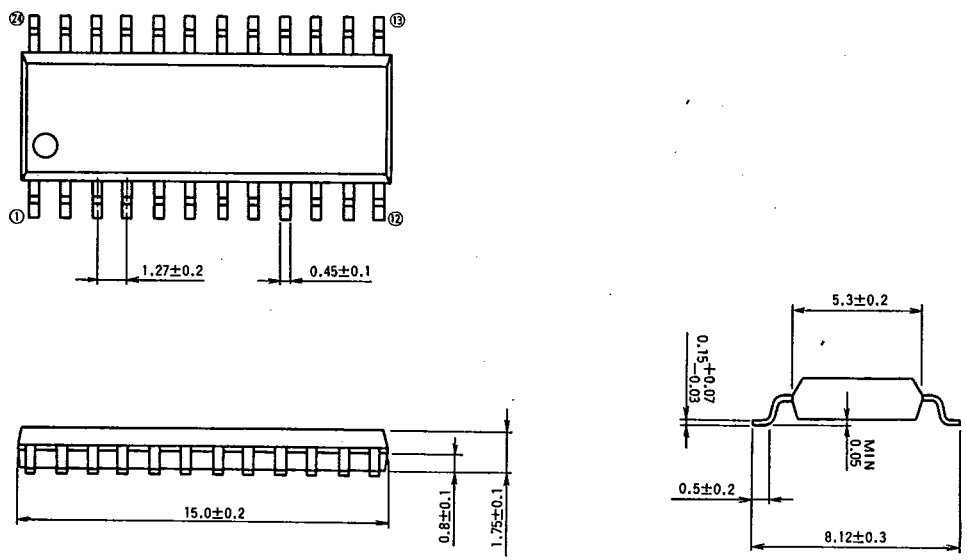
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



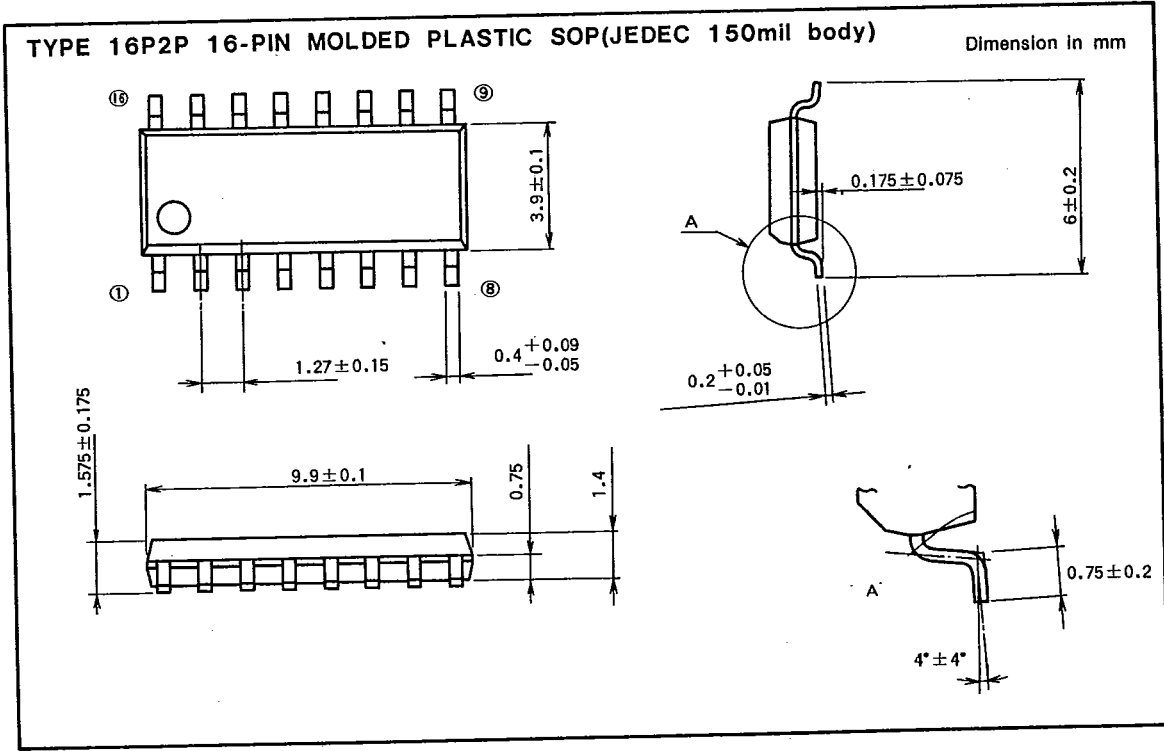
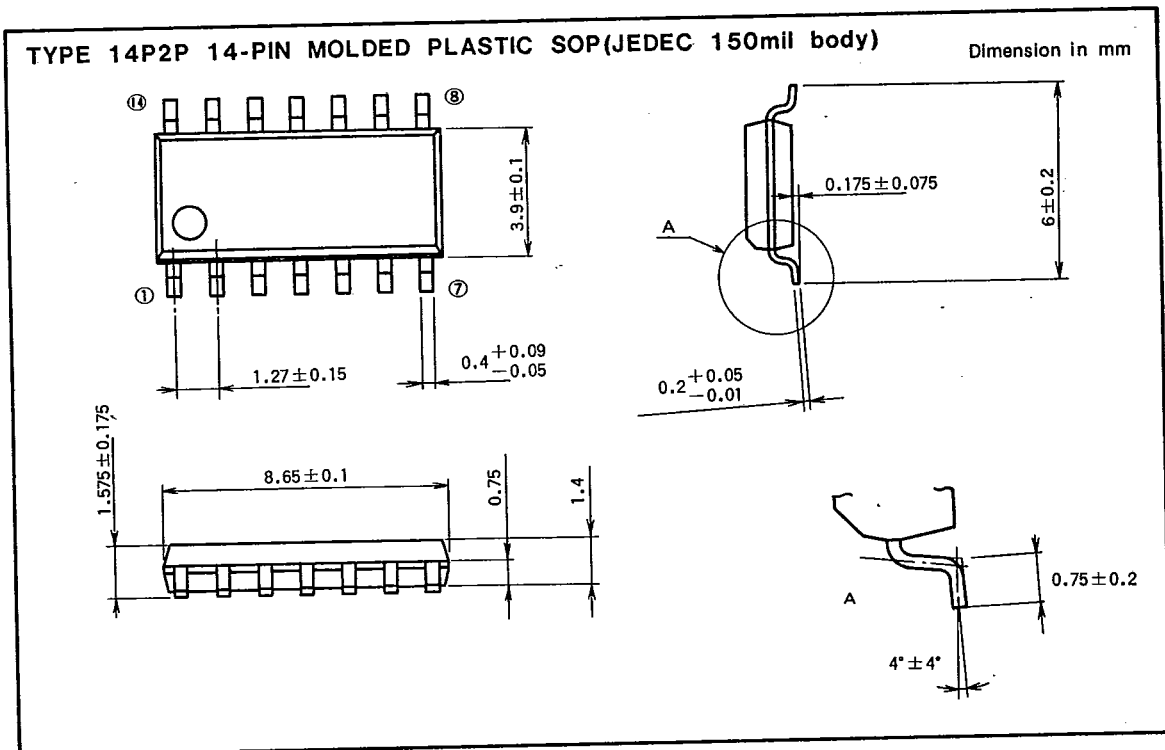
TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm



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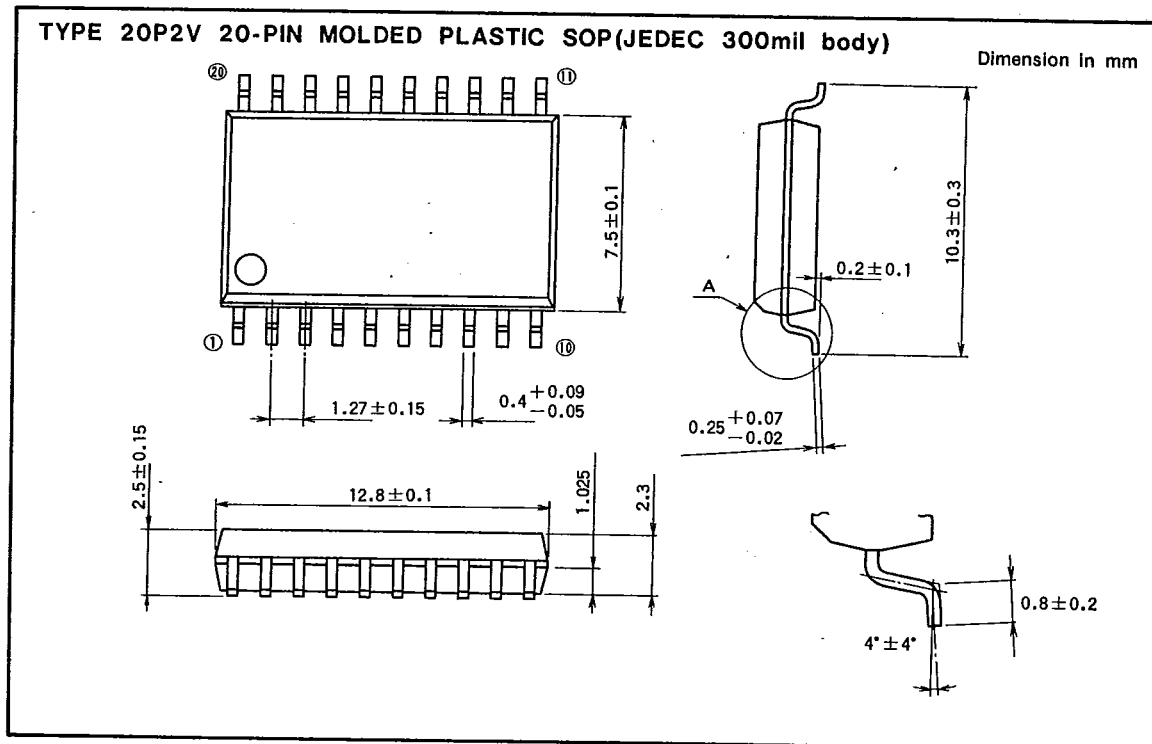
91D 12853 D T90-20



MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12854 D T-90-20



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