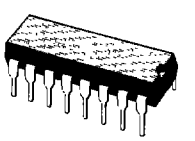
SGS-THOMSON
MICROELECTRONICS

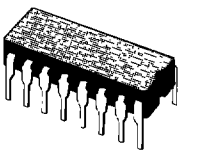
T74LS168
T74LS169

SYNCHRONOUS BI-DIRECTIONAL COUNTERS
LS168-BCD DECADE LS169-MODULO 16 BINARY

- LOW POWER DISSIPATION 100 mW TYPICAL
- HIGH SPEED COUNT FREQUENCY 30 MHz TYPICAL
- FULLY SYNCHRONOUS OPERATION
- FULL CARRY LOOKAHEAD FOR EASY CASCADING
- SINGLE UP/DOWN CONTROL INPUT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE
- POSITIVE EDGE-TRIGGER OPERATION

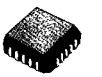


B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)



C1
(Plastic Chip Carrier)

ORDER CODES :

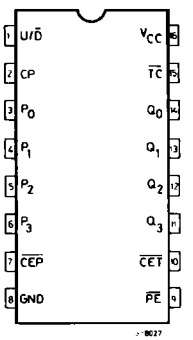
T74LSXXX D1	T74LSXXX C1
T74LSXXX B1	T74LSXXX M1

DESCRIPTION

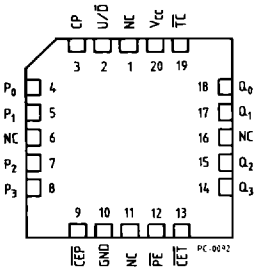
The T74LS168 and T74LS169 are fully synchronous 4-stage up/down counters featuring a present capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. The T54LS/T74LS168 counts in a BCD decade (8, 4, 2, 1) sequence, while the T54LS/T74LS169 operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (Pn → Qn)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (hold)
H	X	H	X	No Change (hold)

H = HIGH Volyge Level
L = LOW Voltage Level
X = Don't Care

PIN NAMES

$\overline{CEP}$	COUNT ENABLE PARALLEL (active LOW) INPUT
$\overline{CET}$	COUNT ENABLE TRICKLE (active LOW) INPUT
CP	CLOCK PULSE (active positive going edge) INPUT
$\overline{PE}$	PARALLEL ENABLE (active LOW) INPUT
U/$\overline{D}$	UP-DOWN COUNT CONTROL INPUT
P_0 - P_3	PARALLEL DATA INPUTS
Q_0 - Q_3	FLIP-FLOP OUTPUTS
$\overline{TC}$	TERMINAL COUNT (active LOW) OUTPUT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

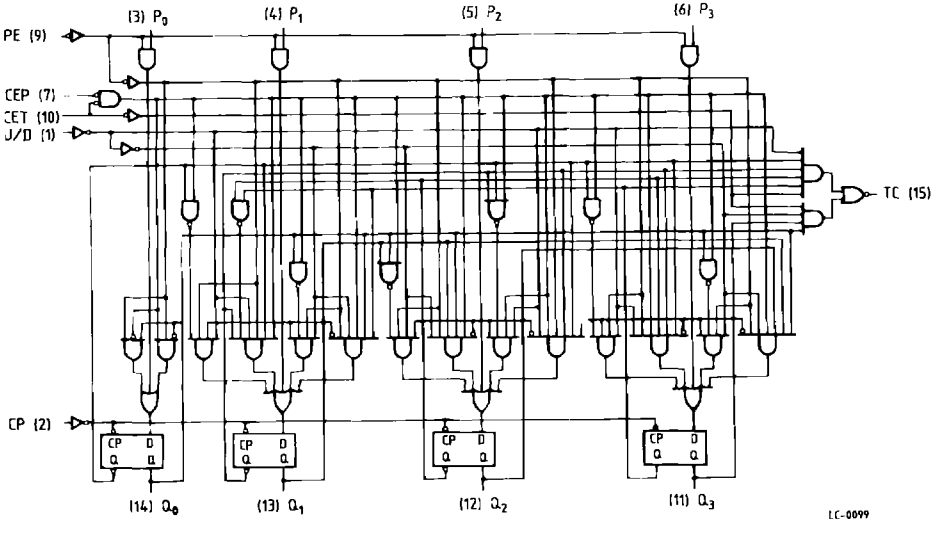
GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS1668/169XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

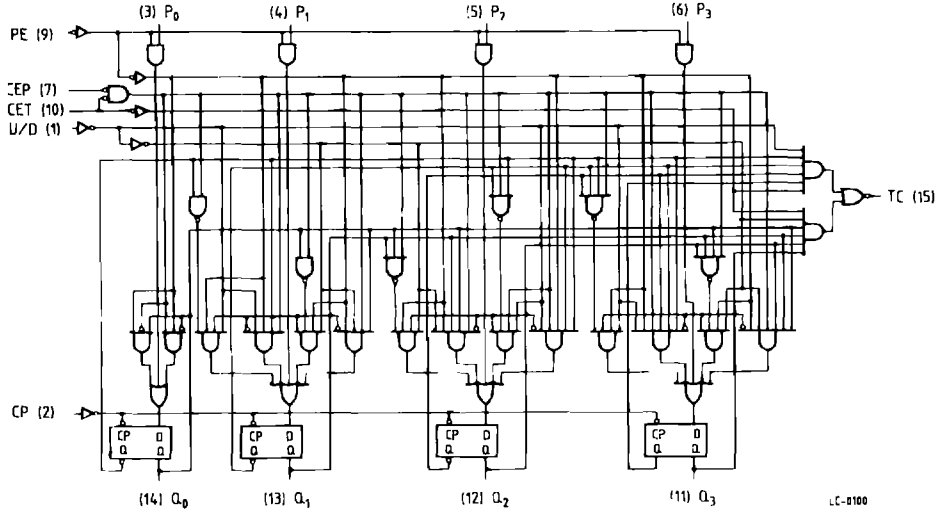
XX = package type.

LOGIC DIAGRAM

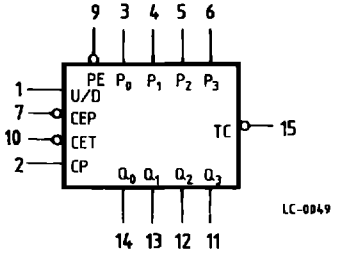
LS168



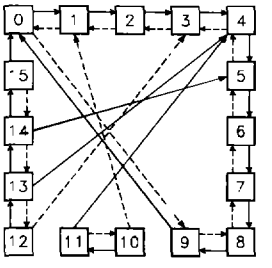
LS169



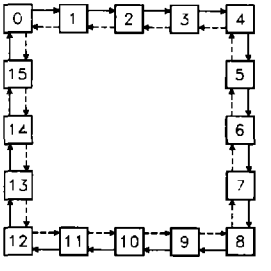
LOGIC SYMBOL AND STATE DIAGRAMS



74LS168
UP/DOWN DECADE COUNTER



74LS169



LS168
UP : $TC = Q_0 \bullet \overline{Q}_3 \bullet (U/\overline{D})$
DOWN : $TC = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (U/D)$
LS169
UP : $TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (U/\overline{D})$
DOWN : $TC = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (U/\overline{D})$

——→ Count up
----------> Count down

FUNCTIONAL DESCRIPTION

The LS168 and LS169 use edge-triggered D-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operation, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flips on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW an $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input the, determines the direction of counting.

The terminal count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the T54LS/T74LS168) in the COUNT UP mode. The TC output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the LS168 decade counter can alsobeLOW in the illegal states 11.13 and via parallel loading. If an illegal state occurs, the LS168 will return to the legitmate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exist the possibility of decoding to spikes on $\overline{TC}$. For this reasons the use of $\overline{TC}$ as a clock signal is not recommended.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current $\overline{U/D}$, CP, $\overline{CEP}$, P_0-P_3, $\overline{PE}$ $\overline{CET}$			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current $\overline{U/D}$, CP, $\overline{CEP}$, P_0-P_3, $\overline{PE}$ $\overline{CET}$			 0.4 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current $\overline{U/D}$, CP, $\overline{CEP}$, P_0-P_3, $\overline{PE}$ $\overline{CET}$			 - 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		20	34	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	CP to Q		15 15	20 20	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	CP to $\overline{TC}$		22 22	30 30	Fig. 3		ns
t_{PLH} t_{PHL}	$\overline{CET}$ to $\overline{TC}$		10 15	15 20	Fig. 2		ns
t_{PLH} t_{PHL}	$\overline{U/D}$ to $\overline{TC}$		20 20	25 25	Fig. 6		ns
f_{MAX}	Maximum Clock Frequency	25	32		Fig. 1		MHz

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
$t_s(L)$ $t_s(H)$	Set-up LOW, Data to CP Set-up HIGH, Data to CP	15 15	12 12		Fig. 4	V_{CC} = 5.0 V	ns
$t_h(L)$ $t_h(H)$	Hold LOW, Data to CP Hold HIGH, Data to CP	5.0 5.0	0 0		Fig. 4		ns
$t_s(L)$ $t_s(H)$	Set-up LOW, $\overline{PE}$ to CP Set-up HIGH, $\overline{PE}$ to CP	15 15	12 12		Fig. 5		ns
$t_h(L)$ $t_h(H)$	Hold LOW, $\overline{PE}$ to CP Hold HIGH, $\overline{PE}$ to CP	5.0 5.0	0 0		Fig. 5		ns
$t_s(L)$ $t_s(H)$	Set-up LOW, $\overline{CET}$ or $\overline{CEP}$ to CP Set-up HIGH, $\overline{CET}$ or $\overline{CEP}$ to CP	 15 15	 12 12		Fig. 5		ns
$t_h(L)$ $t_h(H)$	Hold LOW, $\overline{CET}$ or $\overline{CEP}$ to CP Hold HIGH, $\overline{CET}$ or $\overline{CEP}$ to CP	 15 15	 12 12		Fig. 5		ns
$t_s(L)$ $t_s(H)$	Set-up LOW, U/$\overline{D}$ to CP Set-up HIGH, U/$\overline{D}$ to CP	25 25	20 20		Fig. 6		ns
$t_h(L)$ $t_h(H)$	Hold LOW, U/$\overline{D}$ to CP Hold HIGH, U/$\overline{D}$ to CP	0 0	− 4.0 − 4.0		Fig. 6		ns
t_wCP(L) t_wCP(H)	Clock Pulse Width LOW Clock Pulse Width HIGH	20 10	18 5.0		Fig. 1		ns

DEFINITION OF TERMS

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognizeed and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

Figure 1 : Clock to Output Delays, Count Frequency, and Clock Pulse Width.

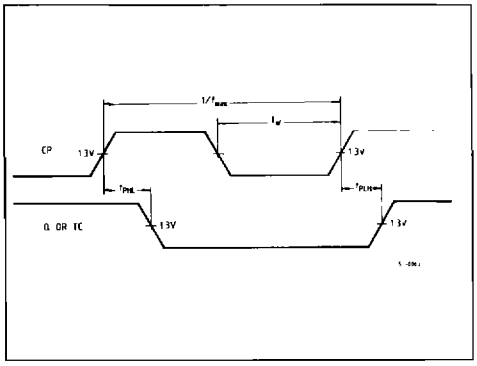


Figure 2 : Count Enable Trickle Input To Terminal Count Output Delays.

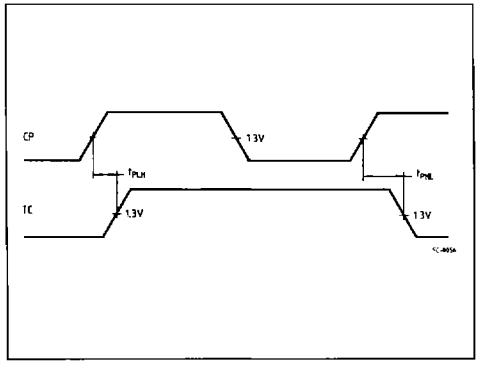


Figure 3 : Clock to Terminal Delays.

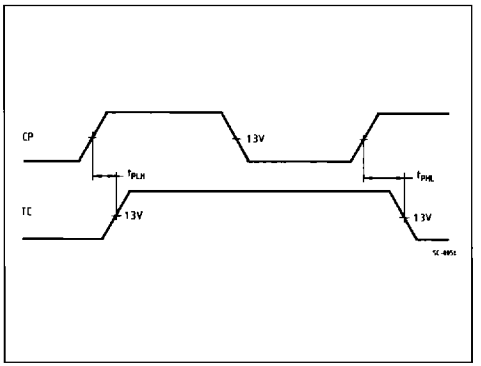


Figure 4 : Set-Up Time (t_s) and Hold (t_h) for Parallel Data Inputs.

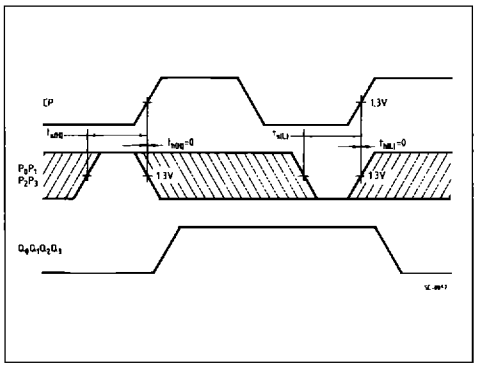
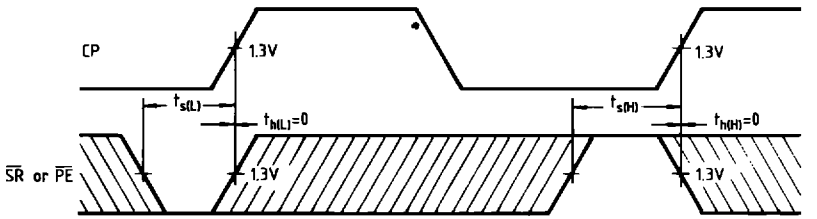


Figure 5 : Set-Up Time (t_s) and Hold Time (t_h) for Count Enable (CEP) and (CET), Parallel Enable (PE) Inputs, and Up-Down (U/D) Control Inputs.



The shaded areas indicate when the input is permitted to change for predictable output performance.

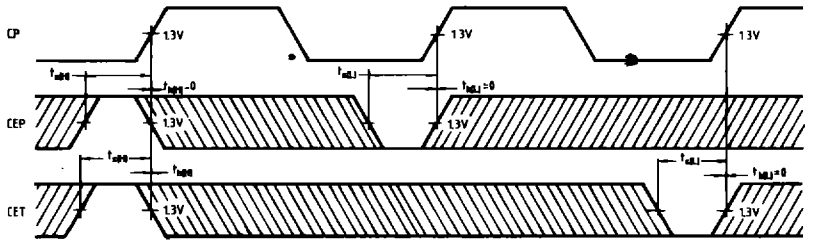


Figure 6 : Up-Down Input to Terminal Count Output Delays.