

TC74HCT564AP/AF TC74HCT574AP/AF

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74HCT564AP/AF **INVERTING**
TC74HCT574AP/AF **NON-INVERTING**

The TC74HCT564A and HCT574A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

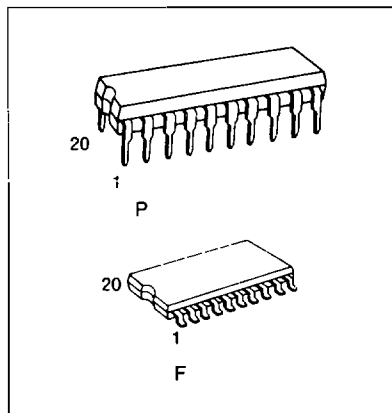
These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input (OE).

The TC74HCT564A has inverting outputs, and the TC74HCT574A has non-inverting outputs.

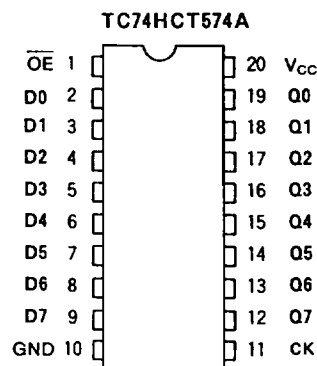
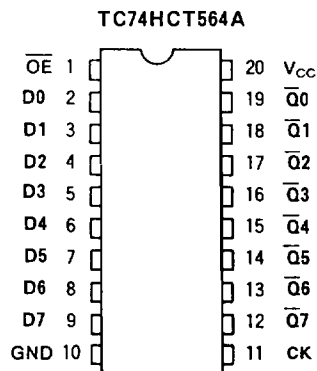
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed $f_{MAX} = 62\text{MHz(Typ.)}$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation $I_{CC} = 4\mu\text{A(Max.)}$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs $V_{IH} = 2\text{V(Max.)}$
 $V_{IL} = 0.8\text{V(Min.)}$
- Output Drive Capability 15 LSTTL Loads
- Symmetrical Output Impedance $|I_{OH}| = I_{OL} = 6\text{mA(Min.)}$
- Balanced Propagation Delays $t_{pLH} = t_{pHL}$
- Pin and Function Compatible with 74LS564/574



PIN ASSIGNMENT



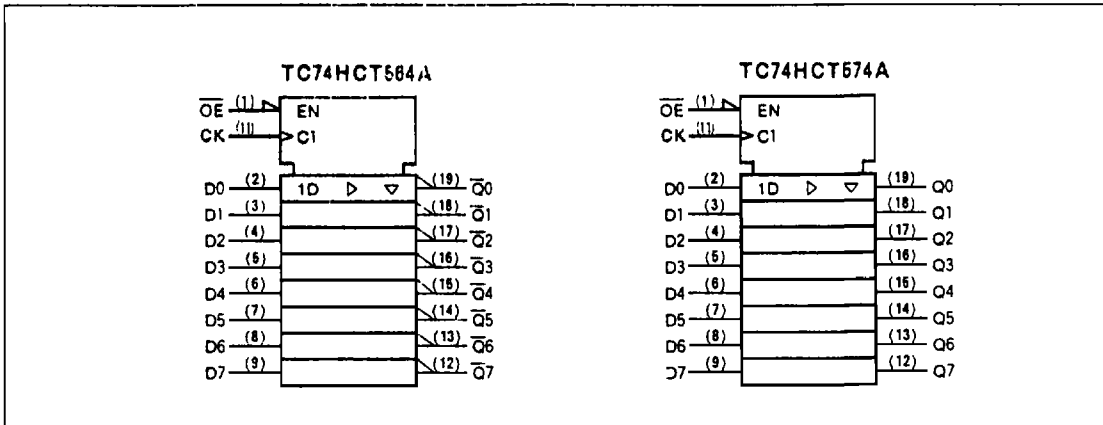
TRUTH TABLE

INPUTS			OUTPUTS	
OE	CK	D	Q(T574A)	Q̄(T564A)
H	X	X	Z	Z
L		X	Q _n	Q̄ _n
L		L	L	H
L		H	H	L

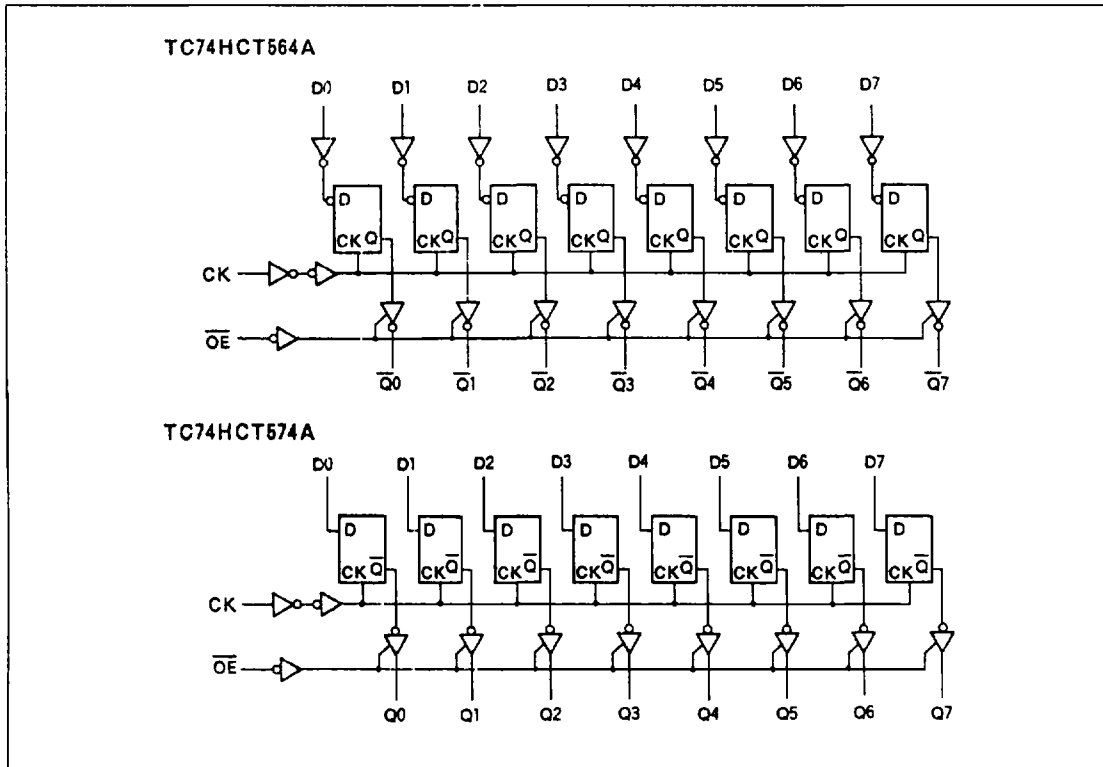
X : Don't Care
Z : High Impedance
Q_n(Q̄_n) : No Change

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IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OLT}	±35	mA
DC V_{CC} /Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{sig}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V_{IH}		4.5	2.0	-	-	2.0	-	V	
			5.5							
Low-Level Input Voltage	V_{IL}		4.5	-	-	0.8	-	0.8	V	
			5.5							
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu\text{A}$	4.5	4.4	4.5	-	4.4	-	V
			$I_{OH} = -6 \text{ mA}$	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu\text{A}$	4.5	-	0.0	0.1	-	0.1	V
			$I_{OL} = 6 \text{ mA}$	4.5	-	0.17	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	-	-	±0.5	-	±5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	μA	
	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	-	-	4.0	-	40.0		
Quiescent Supply Current	ΔI_{CC}	PER INPUT: $V_{IN} = 0.5\text{V}$ or 2.4V OTHER INPUT: V_{CC} or GND	5.5	-	-	2.0	-	2.9	mA	

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TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C		Ta=-40 ~85°C		UNIT
				TYP.	LIMIT	LIMIT		
Minimum Pulse Width (CK)	$t_{W(1D)}$ $t_{W(L)}$		4.5	-	15	19	ns	
			5.5	-	14	17		
Minimum Set-up Time (Dn)	t_s		4.5	-	15	19	ns	
			5.5	-	14	17		
Minimum Hold Time (Dn)	t_h		4.5	-	0	0	ns	
			5.5	-	0	0		
Clock Frequency	f		4.5	-	31	25	MHz	
			5.5	-	34	27		

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25°C			Ta=-40 ~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{TIL}		50	4.5	-	7	12	-	15	ns
				5.5	-	6	11	-	14	
Propagation Delay Time (CK-Q, Q)	t_{pLH} t_{pHL}		50	4.5	-	19	30	-	38	ns
				5.5	-	16	27	-	34	
			150	4.5	-	24	40	-	48	
				5.5	-	21	35	-	44	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1 k\Omega$	50	4.5	-	19	30	-	38	ns
				5.5	-	16	27	-	34	
			150	4.5	-	24	40	-	48	
				5.5	-	21	35	-	44	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1 k\Omega$	50	4.5	-	19	30	-	38	ns
				5.5	-	16	27	-	34	
Maximum Clock Frequency	f_{MAX}		50	4.5	31	50	-	25	-	ns
				5.5	34	60	-	27	-	
Input Capacitance	C_{IN}				-	5	10	-	10	pF
Output Capacitance	C_{OUT}				-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD}(1)$	TC74HCT564A			-	65	-	-	-	
		TC74HCT574A			-	62	-	-	-	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(OPP)} = C_{PD} \cdot V_{CC} \cdot f_N + I_{CC} / 8(\text{per bit})$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 51 + 14 \cdot n(\text{TC74HCT564A})$$

$$C_{PD}(\text{total}) = 47 + 15 \cdot n(\text{TC74HCT574A})$$

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