

## 74AC74 • 74ACT74 Dual D-Type Positive Edge-Triggered Flip-Flop

### General Description

The AC/ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

### Features

- $I_{CC}$  reduced by 50%
- Output source/sink 24 mA
- ACT74 has TTL-compatible inputs

### Ordering Code:

Order Number	Package Number	Package Description
74AC74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC74SC_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC74SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC74MTCX_NL (Note 2)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT74SC_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT74SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT74SJX_NL (Note 2)	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

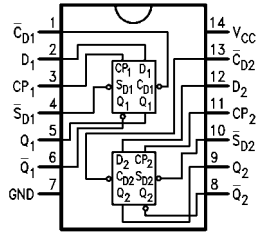
**Note 1:** "\_NL" indicates lead-free product (per JEDEC J-STD-020B).

**Note 2:** "\_NL" indicates lead-free product (per JEDEC J-STD-020B). Device is available in Tape and Reel only.

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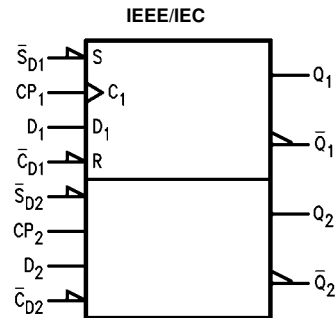
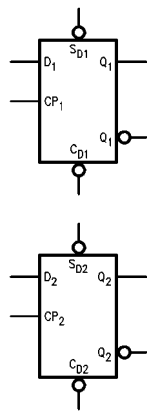
### Connection Diagram



### Pin Descriptions

Pin Names	Description
D <sub>1</sub> , D <sub>2</sub>	Data Inputs
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs
C <sub>D1</sub> , C <sub>D2</sub>	Direct Clear Inputs
S <sub>D1</sub> , S <sub>D2</sub>	Direct Set Inputs
Q <sub>1</sub> , Q <sub>1</sub> $\bar{}$ , Q <sub>2</sub> , Q <sub>2</sub> $\bar{}$	Outputs

### Logic Symbols



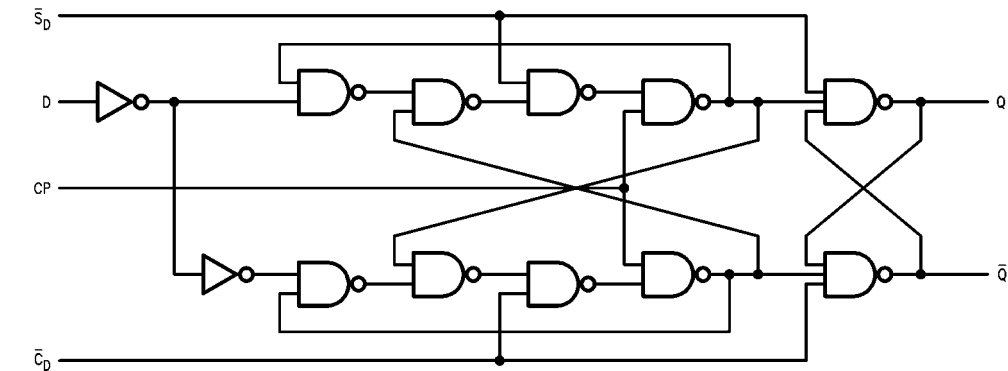
### Truth Table

(Each Half)

Inputs				Outputs	
S <sub>D</sub> $\bar{}$	C <sub>D</sub> $\bar{}$	CP	D	Q	Q $\bar{}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	Q <sub>0</sub>	Q <sub>0</sub> $\bar{}$

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Clock Transition  
 Q<sub>0</sub> (Q<sub>0</sub> $\bar{}$ ) = Previous Q (Q $\bar{}$ ) before LOW-to-HIGH Transition of Clock

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 3)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 3:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-  
out exception, to ensure that the system design is reliable over its power  
supply, temperature, and output/input loading variables. Fairchild does not  
recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics for AC**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits	Typ	Guaranteed Limits		
$V_{IH}$	Minimum HIGH	3.0	1.5	2.1	2.1			V $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
	Level Input	4.5	2.25	3.15	3.15			
	Voltage	5.5	2.75	3.85	3.85			
$V_{IL}$	Maximum LOW	3.0	1.5	0.9	0.9			V $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
	Level Input	4.5	2.25	1.35	1.35			
	Voltage	5.5	2.75	1.65	1.65			
$V_{OH}$	Minimum HIGH	3.0	2.99	2.9	2.9			V $I_{OUT} = -50 \mu A$
	Level Output	4.5	4.49	4.4	4.4			
	Voltage	5.5	5.49	5.4	5.4			
		3.0		2.56	2.46			V $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ m $I_{OH} = -24$ m (Note 4)
		4.5		3.86	3.76			
		5.5		4.86	4.76			
$V_{OL}$	Maximum LOW	3.0	0.002	0.1	0.1			V $I_{OUT} = 50 \mu A$
	Level Output	4.5	0.001	0.1	0.1			
	Voltage	5.5	0.001	0.1	0.1			
		3.0		0.36	0.44			V $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 4)
		4.5		0.36	0.44			
		5.5		0.36	0.44			
$I_{IN}$ (Note 6)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$	
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Maximum	
$I_{OHD}$	Output Current (Note 5)	5.5			-75	mA	$V_{OHD} = 3.85V$ Minimum	
$I_{CC}$ (Note 6)	Maximum Quiescent Supply Current	5.5		2.0	20.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	

**Note 4:** All outputs loaded; thresholds on input associated with output under test.

**Note 5:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 6:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

DC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level Output Voltage	4.5	1.5	0.8	0.8		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4		V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 7)
		5.5		4.86	4.76			
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1		V	I <sub>OUT</sub> = 50 μA
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 7)
		5.5		0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>CC</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	Minimum Dynamic Output Current (Note 8)	5.5			75		mA	V <sub>OLD</sub> = 1.65V Maximum
I <sub>OHD</sub>		5.5			-75		mA	V <sub>OHD</sub> = 3.85V Minimum
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		2.0	20.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
<p><b>Note 7:</b> All outputs loaded; thresholds on input associated with output under test.</p> <p><b>Note 8:</b> Maximum test duration 2.0 ms, one output loaded at a time.</p>								
AC Electrical Characteristics for AC								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>MAX</sub>	Maximum Clock Frequency	3.3	100	125		95		MHz
		5.0	140	160		125		
t <sub>PLH</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3	3.5	8.0	12.0	2.5	13.0	ns
		5.0	2.5	6.0	9.0	2.0	10.0	
t <sub>PHL</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3	4.0	10.5	12.0	3.5	13.5	ns
		5.0	3.0	8.0	9.5	2.5	10.5	
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3	4.5	8.0	13.5	4.0	16.0	ns
		5.0	3.5	6.0	10.0	3.0	10.5	
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q <sub>n</sub>	3.3	3.5	8.0	14.0	3.5	14.5	ns
		5.0	2.5	6.0	10.0	2.5	10.5	
<p><b>Note 9:</b> Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V</p>								

AC Operating Requirements for AC						
Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	Units
			Typ	Guaranteed Minimum		
t <sub>S</sub>	Set-up Time, HIGH or LOW	3.3	1.5	4.0	4.5	ns
	D <sub>n</sub> to CP <sub>n</sub>	5.0	1.0	3.0	3.0	
t <sub>H</sub>	Hold Time, HIGH or LOW	3.3	-2.0	0.5	0.5	ns
	D <sub>n</sub> to CP <sub>n</sub>	5.0	-1.5	0.5	0.5	
t <sub>W</sub>	CP <sub>n</sub> or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3	3.0	5.5	7.0	ns
	Pulse Width	5.0	2.5	4.5	5.0	
t <sub>rec</sub>	Recovery Time	3.3	-2.5	0	0	ns
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	-2.0	0	0	

Note 10: Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

### AC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	5.0	145	210		125		MHz
t <sub>PLH</sub>	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.0	5.5	9.5	2.5	10.5	ns
t <sub>PHL</sub>	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.0	6.0	10.0	3.0	11.5	ns
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	5.0	4.0	7.5	11.0	4.0	13.0	ns
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	5.0	3.5	6.0	10.0	3.0	11.5	ns

Note 11: Voltage Range 5.0 is 5.0V ± 0.5V

### AC Operating Requirements for ACT

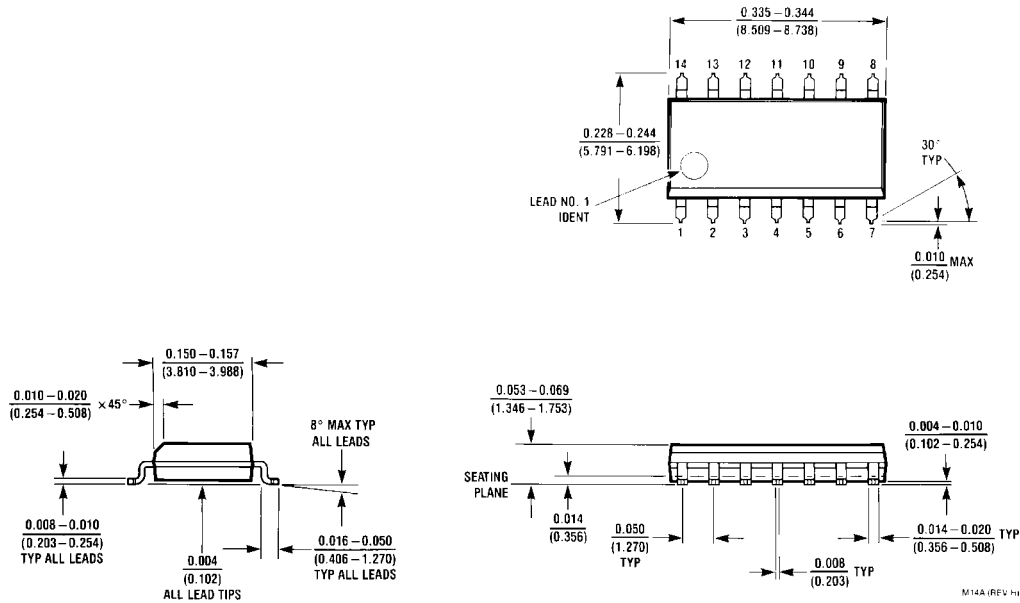
Symbol	Parameter	V <sub>CC</sub> (V) (Note 12)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	Units
			Typ	Guaranteed Minimum		
t <sub>S</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	1.0	3.0	3.5	ns
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	-0.5	1.0	1.0	ns
t <sub>W</sub>	CP <sub>n</sub> or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	6.0	ns
t <sub>rec</sub>	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	-2.5	0	0	ns

Note 12: Voltage Range 5.0 is 5.0V ± 0.5V

### Capacitance

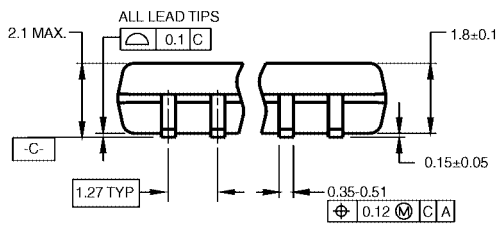
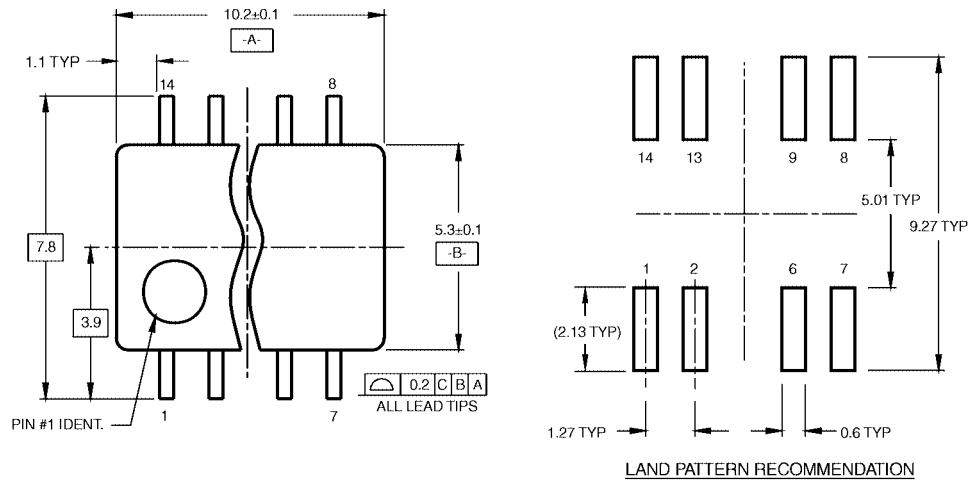
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	35.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**

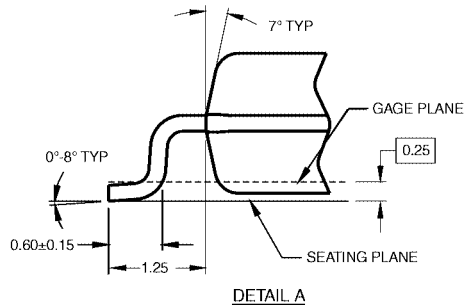
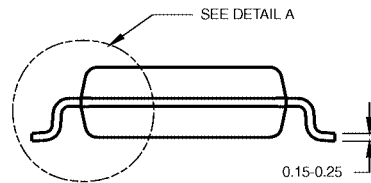
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

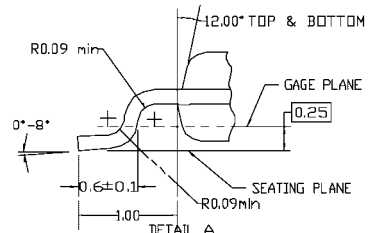
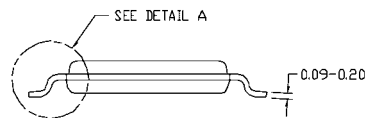
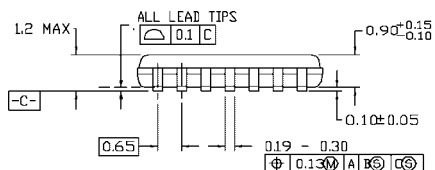
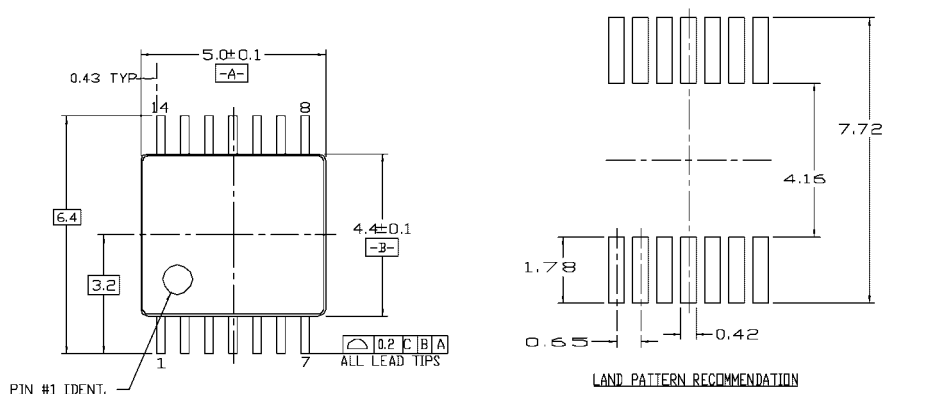
M14DRevB1



**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M14D**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

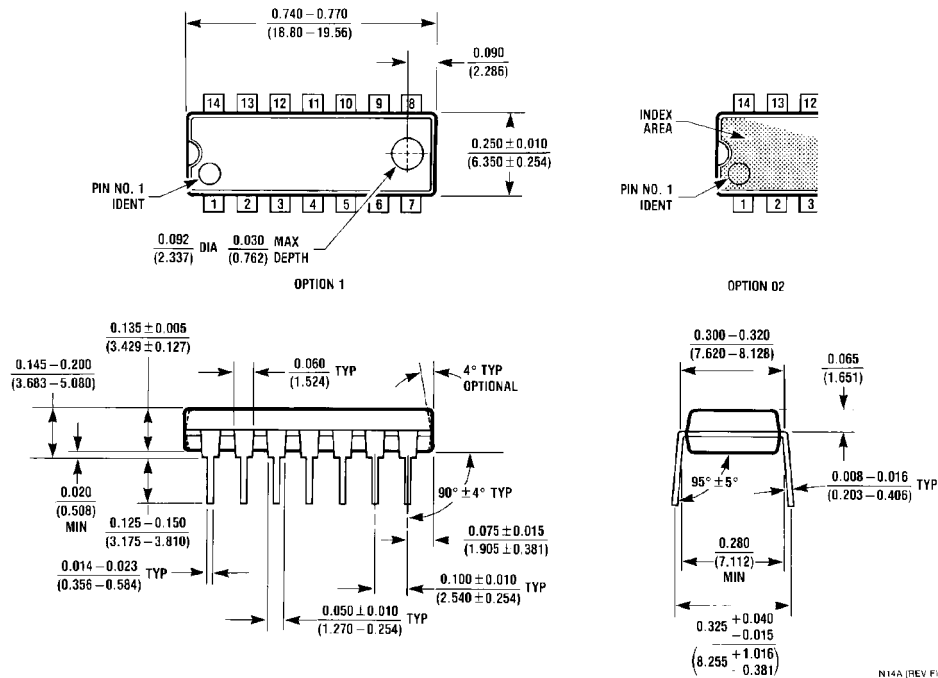


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
  - B. DIMENSIONS ARE IN MILLIMETERS
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
  - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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