# MC14561B

# 9's Complementer

The MC14561B 9's complementer is a companion to the MC14560B NBCD adder to allow BCD subtraction. A BCD number (8–4–2–1 code) is applied to the inputs ($A1 = 2^0$, $A2 = 2^1$, $A3 = 2^2$, $A4 = 2^3$). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable ($\overline{Comp}$) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

When the MC14561B is used to perform BCD subtraction in conjunction with the MC14560B NBCD adder, the complement control becomes an add/subtract control.

- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

**MAXIMUM RATINGS*** (Voltages Referenced to $V_{SS}$)

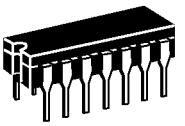
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | – 0.5 to + 18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage (DC or Transient) | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient), per Pin | ± 10 | mA |
| $P_D$ | Power Dissipation, per Package† | 500 | mW |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature (8–Second Soldering) | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

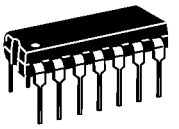
**TRUTH TABLE**

| Z | Comp | $\overline{Comp}$ | F1 | F2 | F3 | F4 | Mode |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | A1 | A2 | A3 | A4 | Straight–through |
| 0 | 0 | 1 | | | | | |
| 0 | 1 | 1 | | | | | |
| 0 | 1 | 0 | $\overline{A}1$ | A2 | $A2\overline{A}3 + \overline{A}2A3$ | $\overline{A}2\overline{A}3\overline{A}4$ | Complement |
| 1 | X | X | 0 | 0 | 0 | 0 | Zero |

X = Don't Care.



**L SUFFIX**
CERAMIC
CASE 632



**P SUFFIX**
PLASTIC
CASE 646

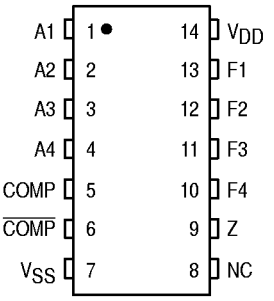
**D SUFFIX**
SOIC
CASE 751A

**ORDERING INFORMATION**

| | |
|---|---|
| MC14XXXBCP | Plastic |
| MC14XXXBCL | Ceramic |
| MC14XXXBD | SOIC |

$T_A$ = – 55° to 125°C for all packages.

**PIN ASSIGNMENT**




NC = NO CONNECTION

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | – 55°C Min | – 55°C Max | 25°C Min | 25°C Typ # | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage "0" Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| "1" Level<br>$V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage "0" Level | $V_{IL}$ | | | | | | | | | Vdc |
| ($V_O$ = 4.5 or 0.5 Vdc) | | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | |
| ($V_O$ = 9.0 or 1.0 Vdc) | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| ($V_O$ = 13.5 or 1.5 Vdc) | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| "1" Level | $V_{IH}$ | | | | | | | | | Vdc |
| ($V_O$ = 0.5 or 4.5 Vdc) | | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | |
| ($V_O$ = 1.0 or 9.0 Vdc) | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| ($V_O$ = 1.5 or 13.5 Vdc) | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Current | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | – 3.0 | — | – 2.4 | – 4.2 | — | – 1.7 | — | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | – 0.64 | — | – 0.51 | – 0.88 | — | – 0.36 | — | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | – 1.6 | — | – 1.3 | – 2.25 | — | – 0.9 | — | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | – 4.2 | — | – 3.4 | – 8.8 | — | – 2.4 | — | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | |
| Input Current | $I_{in}$ | 15 | — | ±0.1 | — | ±0.00001 | ±0.1 | — | ±1.0 | µAdc |
| Input Capacitance<br>($V_{in}$ = 0) | $C_{in}$ | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current<br>(Per Package) | $I_{DD}$ | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | µAdc |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | |
| Total Supply Current**†<br>(Dynamic plus Quiescent, Per Package)<br>($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0 | $I_T$ = (1.5 µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| | | 10 | $I_T$ = (3.0 µA/kHz) f + $I_{DD}$ | | | | | | | |
| | | 15 | $I_T$ = (4.5 µA/kHz) f + $I_{DD}$ | | | | | | | |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

** The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in µA (per package), $C_L$ in pF, V = ($V_{DD}$ – $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.004.

**SWITCHING CHARACTERISTICS*** ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ | Min | Typ # | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$, | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | $t_{THL}$ | 5.0 | — | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | — | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | — | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$, | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 315 ns | $t_{PHL}$ | 5.0 | — | 400 | 1000 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 127 ns | | 10 | — | 160 | 400 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 95 ns | | 15 | — | 120 | 300 | |

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

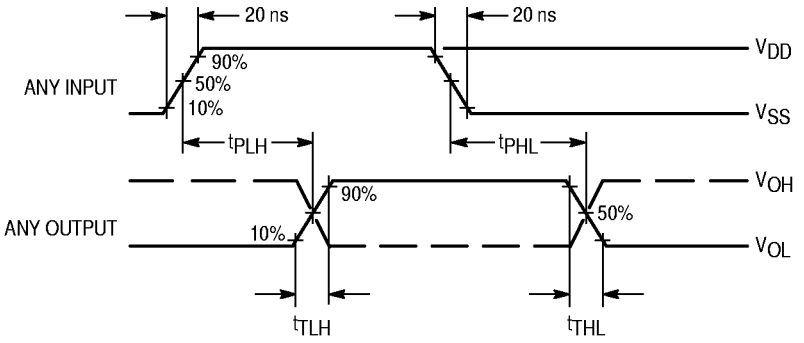
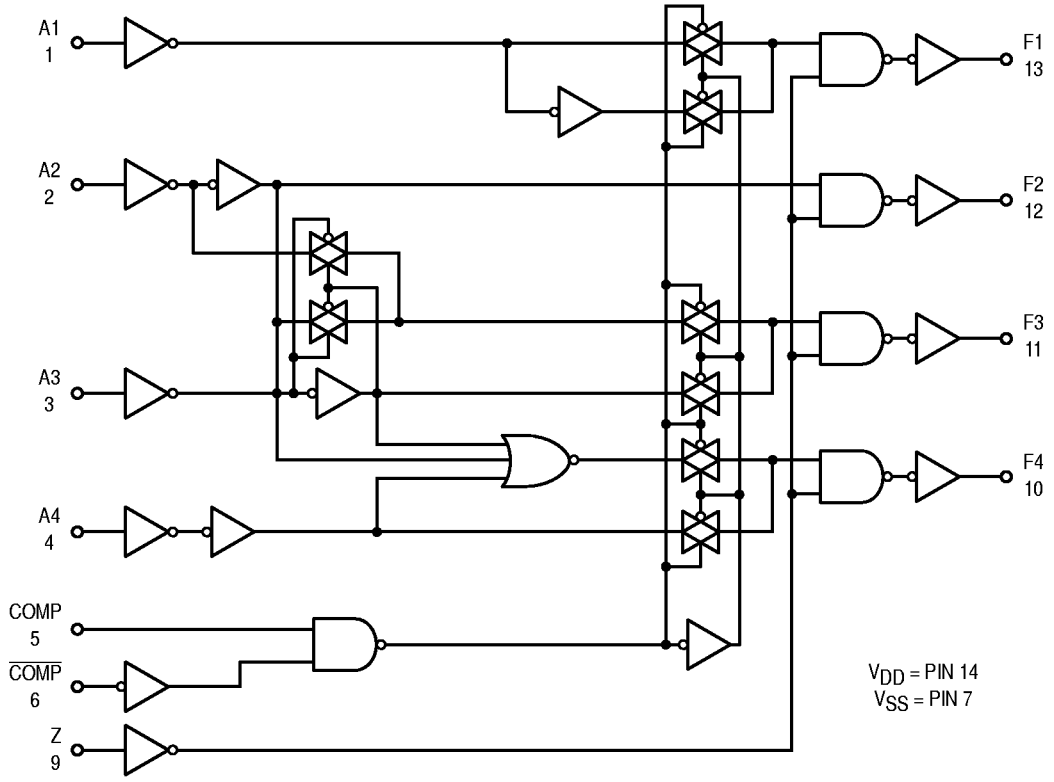



**Figure 1. Switching Time Waveforms**

## LOGIC DIAGRAM



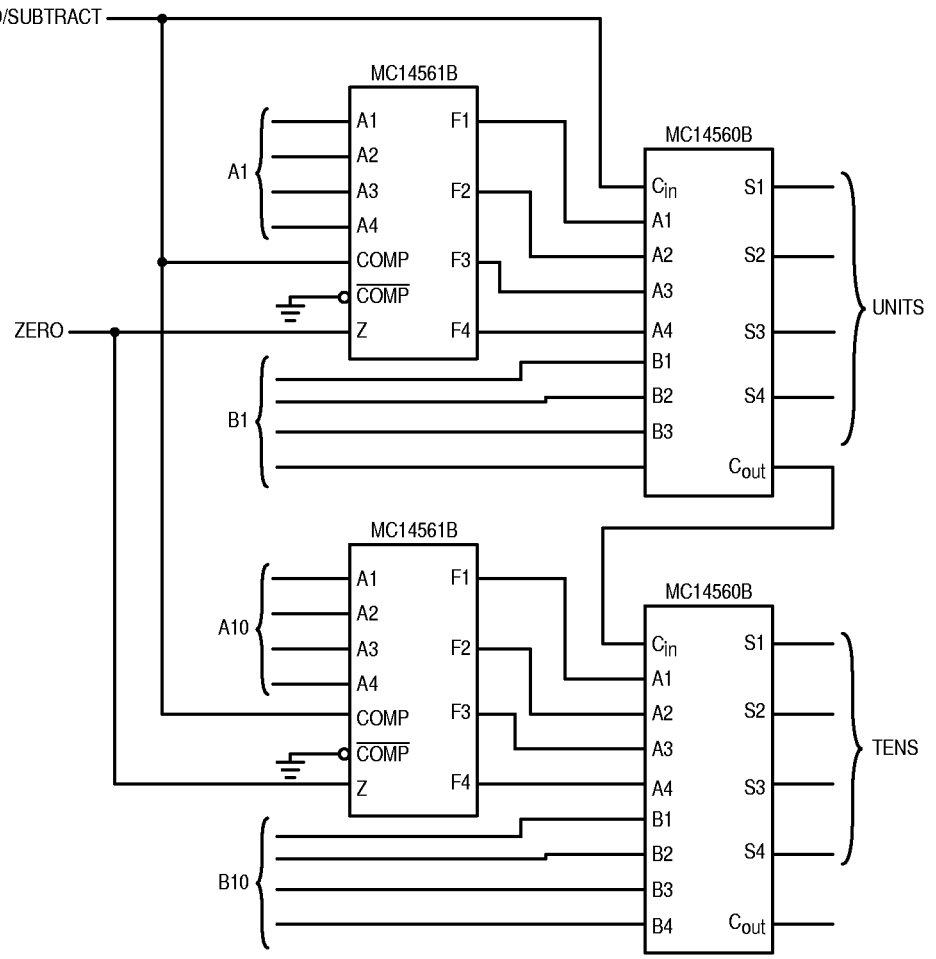

## TRUTH TABLE – COMPLEMENT MODE

(Z = 0, Comp = 1, $\overline{\text{Comp}}$ = 0)

| | Decimal Equivalent Input | Inputs | | | | Decimal Equivalent Output | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | A4 | A3 | A2 | A1 | | F4 | F3 | F2 | F1 |
| | 0 | 0 | 0 | 0 | 0 | 9 | 1 | 0 | 0 | 1 |
| | 1 | 0 | 0 | 0 | 1 | 8 | 1 | 0 | 0 | 0 |
| | 2 | 0 | 0 | 1 | 0 | 7 | 0 | 1 | 1 | 1 |
| | 3 | 0 | 0 | 1 | 1 | 6 | 0 | 1 | 1 | 0 |
| | 4 | 0 | 1 | 0 | 0 | 5 | 0 | 1 | 0 | 1 |
| | 5 | 0 | 1 | 0 | 1 | 4 | 0 | 1 | 0 | 0 |
| | 6 | 0 | 1 | 1 | 0 | 3 | 0 | 0 | 1 | 1 |
| | 7 | 0 | 1 | 1 | 1 | 2 | 0 | 0 | 1 | 0 |
| | 8 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| | 9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Illegal BCD Input Codes | 10 | 1 | 0 | 1 | 0 | 7 | 0 | 1 | 1 | 1 |
| | 11 | 1 | 0 | 1 | 1 | 6 | 0 | 1 | 1 | 0 |
| | 12 | 1 | 1 | 0 | 0 | 5 | 0 | 1 | 0 | 1 |
| | 13 | 1 | 1 | 0 | 1 | 4 | 0 | 1 | 0 | 0 |
| | 14 | 1 | 1 | 1 | 0 | 3 | 0 | 0 | 1 | 1 |
| | 15 | 1 | 1 | 1 | 1 | 2 | 0 | 0 | 1 | 0 |

## TYPICAL APPLICATIONS

One MC14560B and one MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.




**TRUTH TABLE**

| Zero | Add/Subtract | Result |
|---|---|---|
| 0 | 0 | B plus A |
| 0 | 1 | B minus A |
| 1 | X | B |

X = Don't Care

**Figure 2. Parallel Add/Subtract Circuit (10's Complement)**

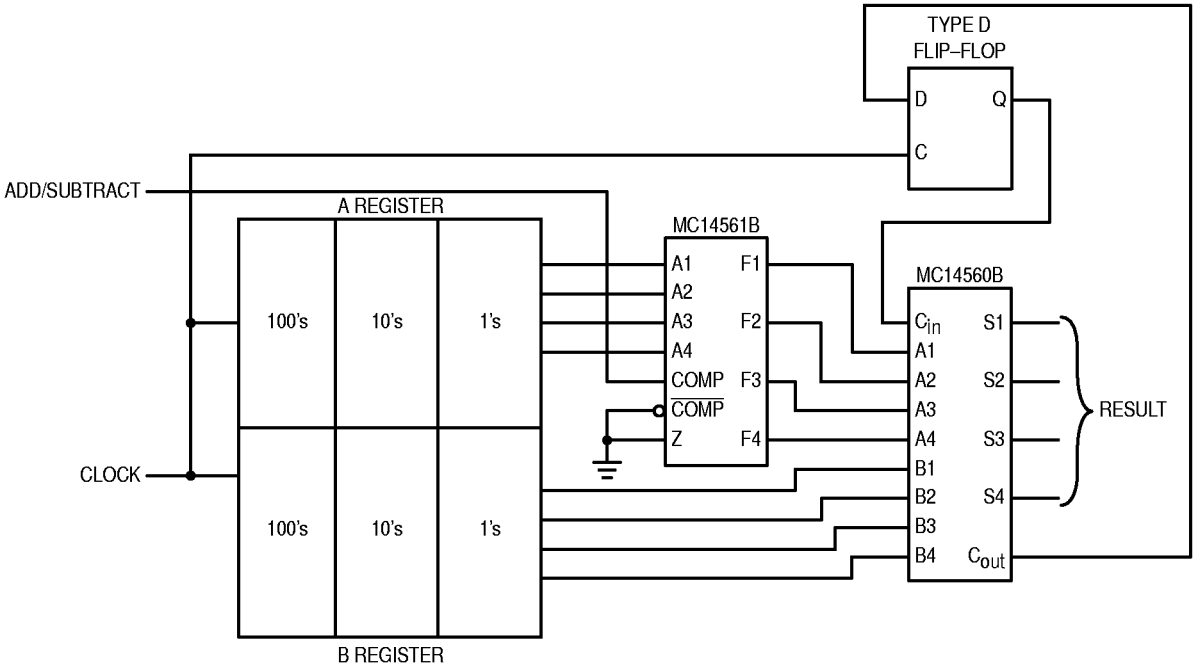
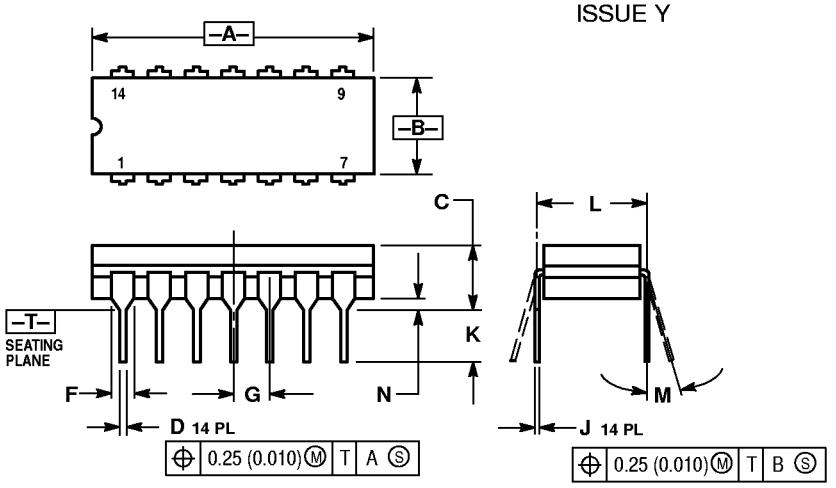



**Figure 3. Serial Add/Subtract Circuit**

## OUTLINE DIMENSIONS

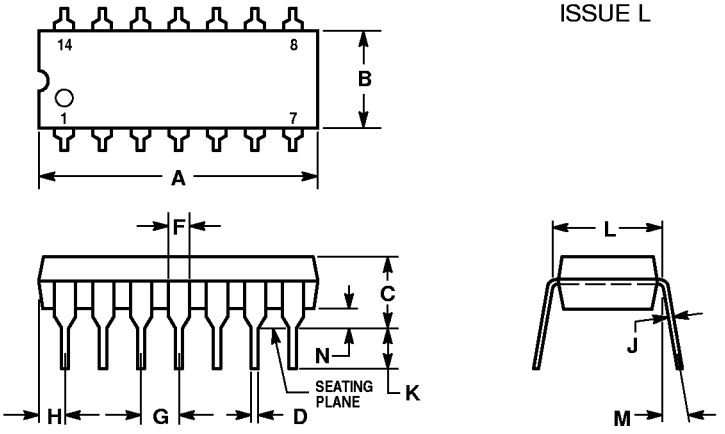
**L SUFFIX**
CERAMIC DIP PACKAGE
CASE 632–08
ISSUE Y




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.94 |
| B | 0.245 | 0.280 | 6.23 | 7.11 |
| C | 0.155 | 0.200 | 3.94 | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**P SUFFIX**
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L

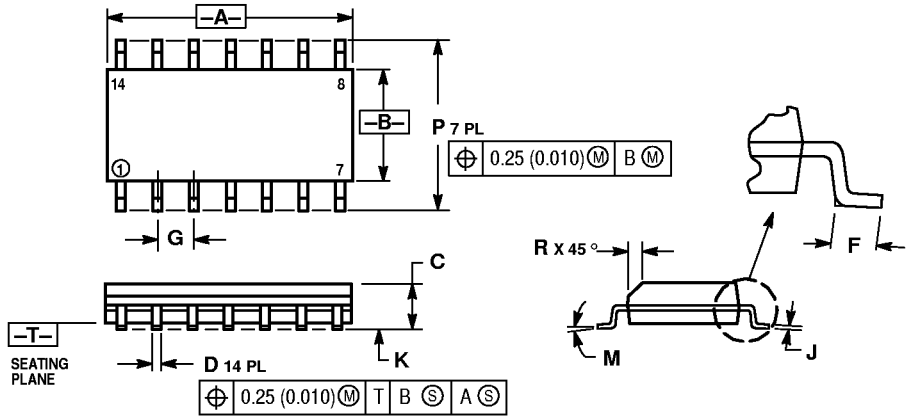



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.015 | 0.039 | 0.39 | 1.01 |

## OUTLINE DIMENSIONS

**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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