

DATA SHEET

SURFACE MOUNT MULTILAYER CERAMIC CAPACITORS

LOW ACOUSTIC NOISE MLCC

X5R/X7R

6.3 V TO 50 V 100nF to 10 μF

RoHS compliant & Halogen free



YAGEO Phicomp



SCOPE

This specification describes X5R/X7R series chip capacitors with lead-free terminations.

YAGEO Phicomp

APPLICATIONS

PCs, Hard disk, Game PCs Power supplies **DVD** players Mobile phones Data processing

FEATURES

Supplied in tape on reel Nickel-barrier end termination RoHS compliant Halogen free compliant

ORDERING INFORMATION-GLOBAL PART NUMBER, PHYCOMP

CTC

All part numbers are identified by the series, size, tolerance, TC material, packing style, voltage, process code, termination and capacitance value.

YAGEO BRAND ordering code

GLOBAL PART NUMBER (PREFERRED)

XXXX X X XXX X BB XXX (1) (2) (3) (4) (5)

(I) SIZE - INCH BASED (METRIC)

0402 (1005)

0805 (2012)

1206 (3216)

(2) TOLERANCE

 $K = \pm 10\%$

 $M = \pm 20\%$

(3) PACKING STYLE

R = Paper/PE taping reel; Reel 7 inch

K = Blister taping reel; Reel 7 inch

P = Paper/PE taping reel; Reel 13 inch

F = Blister taping reel; Reel 13 inch

(4) TC MATERIAL

X5R

(5) RATED VOLTAGE

5 = 6.3 V

6 = 10 V

8 = 25 V

(6) CAPACITANCE VALUE

2 significant digits+number of zeros

The 3rd digit signifies the multiplying factor, and letter R is decimal point

Example: $103 = 10 \times 10^3 = 10,000 \text{ pF} = 10 \text{ nF}$

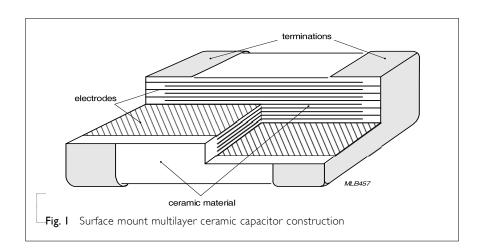




YAGEO Phicomp

The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two end terminations and finally covered with a layer of plated tin (NiSn). Thterminations are lead-free. A cross section of the structure is shown in Fig. I.

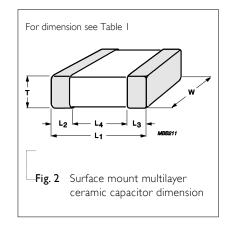


DIMENSION

Table I For outlines see fig. 2

TYPE	L ₁ (mm)	W (mm)	T (MM)	L_2 / L_3	(mm)	L ₄ (mm)
1116	L ₁ (111111)	** (IIIII)	1 (11111)	min.	max.	min.
0402	1.0 ±0.15	0.5 ±0.15	- 5.6	0.20	0.30	0.40
0805	2.0 ±0.20	1.25 ±0.20	Refer to table 2 to 3	0.25	0.75	0.55
1206	3.2 ±0.30	1.6 ±0.30	table 2 to 3	0.25	0.75	1.40

OUTLINES





CAPACITANCE RANGE & THICKNESS FOR X5R

Table 2	Sizes fr	n n n n	I to 1206

YAGEO Phicomp

CAP.	0402	0805	1206
	6.3 V	10 V	25 V
100 nF	-	-	
220 nF			
470 nF			
l uF		1.25 ±0.2	
2.2 uF	0.5 ±0.15	1.25 ±0.2	
4.7 uF		1.25 ±0.2	
IO uF		1.25 ±0.2	1.60 ±0.3

NOTE

- 1. Values in shaded cells indicate thickness class in mm
- 2. Capacitance value of non E-6 series is on request
- 3. For special ordering code, please contact local sales force before order.

THICKNESS CLASSES AND PACKING QUANTITY

Table 4

SIZE	THICKNESS	TAPE WIDTH -	Ø180 M1	1 / 7 INCH	Ø330 MN	1 / 13 INCH	QUANTITY
CODE	CLASSIFICATION	QUANTITY PER REEL	Paper	Blister	Paper	Blister	PER BULK CASE
0402	0.5 ±0.15 mm	8 mm	10,000		50,000		50,000
0805	1.25 ±0.2 mm	8 mm		3,000		10,000	5,000
1206	1.6 ±0.3 mm	8 mm		2,000		8,000	



ELECTRICAL CHARACTERISTICS

YAGEO Phicomp

X5R/X7R DIELECTRIC CAPACITORS; NISN TERMINATIONS

Unless otherwise specified, all tests and measurements shall be made under standard atmospheric conditions for testing as given in 5.3 of IEC 60068-1:

- Temperature: 15 °C to 35 °C - Relative humidity: 25% to 75% - Air pressure: 86 kPa to 106 kPa

Before the measurements are made, the capacitor shall be stored at the measuring temperature for a time sufficient to allow the entire capacitor to reach this temperature.

The period as prescribed for recovery at the end of a test is normally sufficient for this purpose.

Table 5	
DESCRIPTION	VALUE
Capacitance range	luF to 10 μF
Capacitance tolerance	±10% and ±20%
Dissipation factor (D.F.)	
	≤ 10%
Insulation resistance after I minute at U_r (DC)	$R_{ins} \times C_r \ge 100 \ \Omega.F$
Maximum capacitance change as a function of temperature (temperature characteristic/coefficient):	±15%
Operating temperature range:	
X5R	–55 °C to +85 °C



SOLDERING RECOMMENDATION

YAGEO Phicomp

 Гah	le I	16

SOLDERING METHOD	SIZE 0402	0603	0805	1206	≥ 1210
Reflow	≥ 0.1 µF	≥ 1.0 µF	≥ 2.2 µF	≥ 4.7 µF	Reflow only
Reflow/Wave	< 0.1 µF	< 1.0 µF	< 2.2 µF	< 4.7 µF	

TESTS AND REQUIREMENTS

Table 17 Test procedures and requirements

TEST	TEST METHO	D	PROCEDURE	REQUIREMENTS
Mounting	IEC 60384- 21/22	4.3	The capacitors may be mounted on printed-circuit boards or ceramic substrates	No visible damage
Visual Inspection and Dimension Check		4.4	Any applicable method using × 10 magnification	In accordance with specification
Capacitance (1)		4.5.1	Class 2: At 20 °C, 24 hrs after annealing	Within specified tolerance
			f = 1 KHz for C \leq 10 μF , rated voltage > 6.3 V, measuring at voltage 1 V_{rms} at 20 °C	
			$f=$ 1 KHz, for C \leq 10 μF , rated voltage \leq 6.3 V, measuring at voltage 0.5 V_{rms} at 20 $^{\circ} C$	
			$f=$ 120 Hz for C $>$ 10 μF , measuring at voltage 0.5 V_{ms} at 20 $^{\circ} C$	
Dissipation Factor (D.F.) (1)		4.5.2	Class 2: At 20 °C, 24 hrs after annealing	In accordance with specification
			f = 1 KHz for C \leq 10 μF , rated voltage > 6.3 V, measuring at voltage 1 V_{rms} at 20 °C	
			$f=1$ KHz, for C \leq 10 μF , rated voltage \leq 6.3 V, measuring at voltage 0.5 V_{rms} at 20 $^{\circ}C$	
			$f=$ 120 Hz for C $>$ 10 μF , measuring at voltage 0.5 V_{rms} at 20 $^{\circ} C$	
Insulation Resistance		4.5.3	At U _r (DC) for I minute	In accordance with specification

NOTE

 $I.\ The\ figure\ indicates\ typical\ inspection.\ Please\ refer\ to\ individual\ specifications.$



TEST	TEST METHO	DD	PROCEDURE	REQUIREMENTS
Temperature Characteristic		4.6	Capacitance shall be measured by the steps shown in the following table. The capacitance change should be measured after 5 min at each specified temperature stage. Step Temperature(°C) a 25±2 b Lower temperature±3°C c 25±2 d Upper Temperature±2°C e 25±2 (I) Class I Temperature Coefficient shall be calculated from the formula as below Temp, Coefficient = $\frac{C2 - C1}{C1 \times \Delta T} \times 10^6$ [ppm/°C] C1: Capacitance at step c C2: Capacitance at 125°C ΔT : 100 °C(=125°C-25°C) (2) Class II Capacitance Change shall be calculated from the formula as below $\Delta C = \frac{C2 - C1}{C1} \times 100\%$ C1: Capacitance at step c C2: Capacitance at step c	<general purpose="" series=""> Class 1: Δ C/C: ±30ppm Class2: X7R: Δ C/C: ±15% Y5V: Δ C/C: 22~-82% <high capacitance="" series=""> Class2: X7R/X5R: Δ C/C: ±15% Y5V: Δ C/C: 22~-82%</high></general>
Adhesion		4.7	A force applied for 10 seconds to the line joining the terminations and in a plane parallel to the substrate	Force $size \ge 0603: 5N$ size = 0402: 2.5N size = 0201: 1N
Bending Strength	IEC 60384-	4.8	Mounting in accordance with IEC 60384-22 paragraph 4.3	No visible damage
	21/22		Conditions: bending I mm at a rate of I mm/s, radius jig 340 mm	<general purpose="" series=""> ΔC/C Class2: X5R: ±10% <high capacitance="" series=""> ΔC/C Class2: X5R: ±10%</high></general>





Surface Mount Multilayer Ceramic Capacitors Low Acoustic Noise

TEST	TEST METHOD	ı	PROCEDURE	REQUIREMENTS
Resistance to Soldering Heat		4.9	Precondition: 150 +0/ $-$ 10 °C for I hour, then keep for 24 ±1 hours at room temperature Preheating: for size \leq 1206: 120 °C to 150 °C for I	Dissolution of the end face plating shall not exceed 25% of the length of the edge concerned
			minute Preheating: for size > 1206: 100 °C to 120 °C for I minute and 170 °C to 200 °C for I minute Solder bath temperature: 260 ±5 °C Dipping time: 10 ±0.5 seconds Recovery time: 24 ±2 hours	<pre><general purpose="" series=""> ΔC/C Class2: X5R: ±10% </general></pre> <pre><high capacitance="" series=""></high></pre> ΔC/C
				Class2: X5R: ±10%
			•	D.F. within initial specified value R _{ins} within initial specified value
Solderability		4.10	Preheated the temperature of 80 °C to 140 °C and maintained for 30 seconds to 60 seconds.	The solder should cover over 95% of the critical area of each termination
			 Temperature: 235±5°C / Dipping time: 2 ±0.5 s Temperature: 245±5°C / Dipping time: 3 ±0.5 s (lead free) Depth of immersion: 10mm 	
Rapid Change of Temperature	IEC 60384-	4.11	Preconditioning; 150 +0/-10 °C for 1 hour, then keep for 24 ±1 hours at .	No visual damage
·	21/22		room temperature 5 cycles with following detail: 30 minutes at lower category temperature 30 minutes at upper category temperature	<general purpose="" series=""> ΔC/C Class2: X5R: ±15%</general>
			Recovery time 24 ±2 hours	<pre><high capacitance="" series=""> $\Delta C/C$ Class2: X5R: $\pm 15\%$</high></pre>
				D.F. meet initial specified value R _{ins} meet initial specified value

YAGEO Phicomp

whichever is less

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Damp Heat	4.13	Preconditioning, class 2 only:	No visual damage after recovery
with U _r Load		150 +0/-10 °C /1 hour, then keep for 24 \pm 1 hour	<general purpose="" series=""></general>
		at room temp	ΔC/C
		2. Initial measure:	Class2:
		Spec: refer to initial spec C, D, IR	X5R: ±15%
		3. Damp heat test:	D.F.
		500 ± 12 hours at 40 ± 2 °C; $90 \text{ to } 95\%$ R.H. 1.0 U_r applied	Class2:
			X5R: ≤ 16V: ≤ 7%
		4. Recovery: Class 2: 24 ±2 hours	≥ 25V: ≤ 5%
		5. Final measure: C, D, IR	R _{ins}
		5. Final measure. C, D, iii	Class2:
		P.S. If the capacitance value is less than the minimum	$X5R: \ge 500 \text{ M}\Omega \text{ or } R_{\text{ins}} \times C_r \ge 25s$
		value permitted, then after the other measurements	whichever is less
		have been made the capacitor shall be preconditioned according to "IEC 60384 4.1" and then the	<high capacitance="" series=""></high>
		requirements shall be met.	ΔC/C
		1	Class2:
			X5R: ±20%
			D.F.
			Class2:
			X5R: 2 × initial value max
			R _{ins}
			Class2:
			Rins × Cr ≥ 5s



YAGEO Phicomp

TEST	TEST METH	OD	PROCEDURE	REQUIREMENTS
Endurance	IEC 60384- 21/22	4.14	 Preconditioning, class 2 only: 150 +0/-10 °C /1 hour, then keep for 24 ±1 hour at room temp Initial measure: Spec: refer to initial spec C, D, IR Endurance test: Temperature: X5R: 85 °C Specified stress voltage applied for 1,000 hours:	No visual damage
Voltage Proof			Specified stress voltage applied for 1~5 seconds Ur ≤ 50 V: series applied 2.5 Ur Charge/Discharge current less than 50mA	No breakdown or flashover

Product specification

Surface Mount Multilayer Ceramic Capacitors Low Acoustic Noise X5R/X7R 6.3 V to 50 V

REVISION HISTORY

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version 2	Jan. 12, 2016		- Capacitance range & thickness
Version I	Dec. 28, 2015		- Capacitance range & thickness
Version 0	Aug. 19, 2014	-	- New Datasheet

