

## TC74HC160/162AP/AF TC74HC161/163AP/AF/AFN

- Synchronous Presettable 4-Bit Counter**  
**TC74HC160 Decade, Asynchronous Clear**  
**TC74HC161 Binary, Asynchronous Clear**  
**TC74HC162 Decade, Synchronous Clear**  
**TC74HC163 Binary, Synchronous Clear**

The TC74HC160A, 161A, 162A and 163A are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 74HC160A/162A are BCD decade counters and the TC74HC161A/163A are 4 bit binary counters.

The CLOCK input is active on the rising edge. Both LOAD and CLEAR inputs are active on low logic level.

Presetting of all four IC's is synchronous to the rising edge of CLOCK.

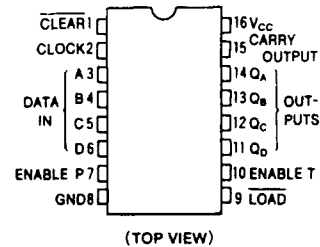
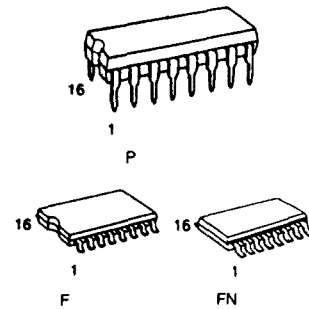
The clear function of the TC74HC162A/163A is synchronous to CLOCK, while the TC74HC160A/161A are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

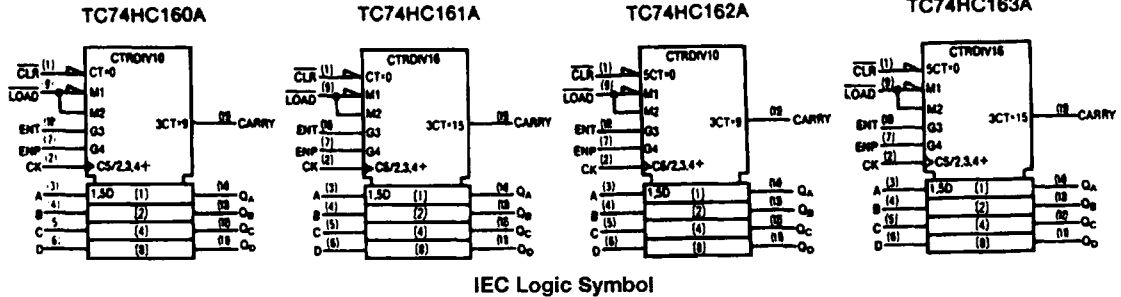
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High Speed:  $t_{MAX} = 63\text{MHz(Typ.)}$  at  $V_{CC} = 5\text{V}$
- Low Power Dissipation:  $I_{CC} = 4\mu\text{A(Max.)}$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%V_{CC}(\text{Min.})$
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance:  $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays:  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range:  $V_{CC}(\text{opr}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS160 ~ 163



Pin Assignment



IEC Logic Symbol

Truth Table

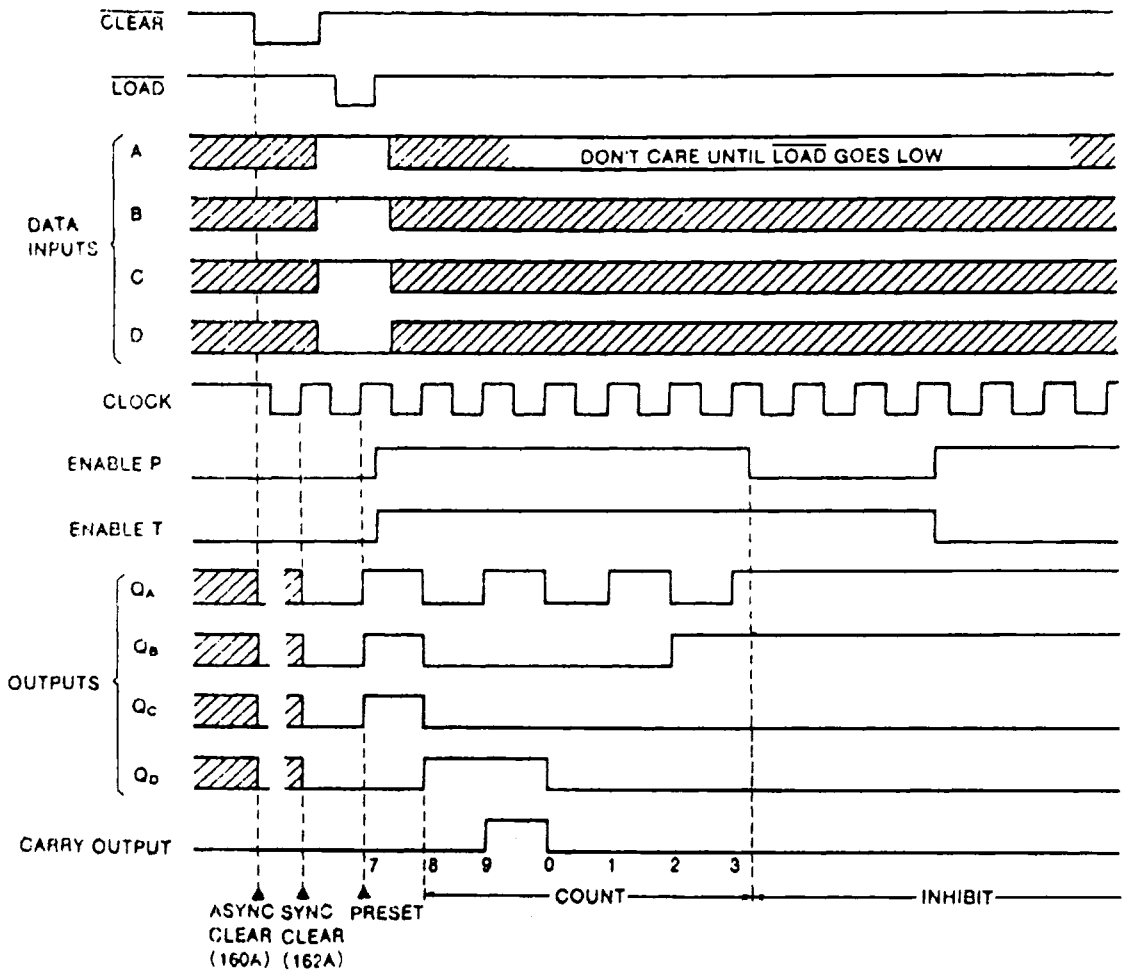
TC74HC160A/161A					TC74HC162A/163A					Outputs				Function
Inputs					Inputs					Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	
CLR	LD	ENP	ENT	CK	CLR	LD	ENP	ENT	CK	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	
L	X	X	X	X	L	X	X	X	↔	L	L	L	L	Reset To "0"
H	L	X	X	↔	H	L	X	X	↔	A	B	C	D	PRESET Data
H	H	X	L	↔	H	H	X	L	↔	No Change				No Count
H	H	L	L	↔	H	H	L	X	↔	No Change				No Count
H	H	H	H	↔	H	H	H	H	↔	Count Up				Count
H	X	X	X	↔	X	X	X	X	↔	No Change				No Count

X: Don't Care

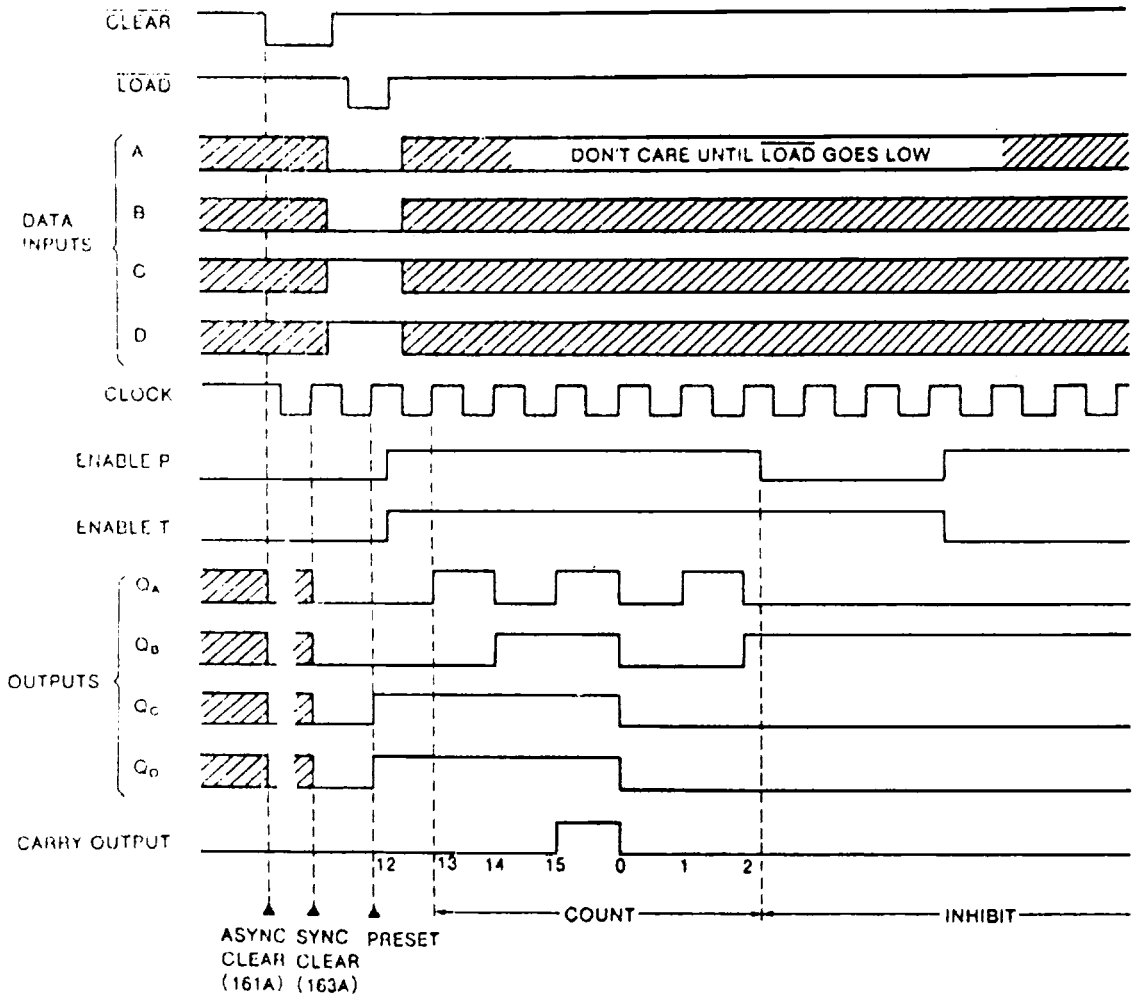
A, B, C, D: Logic Level of Data Inputs

Carry:  $CARRY = ENT \cdot Q_A \cdot \bar{Q}_B \cdot \bar{Q}_C \cdot Q_D \dots$  (TC74HC160A/162A)

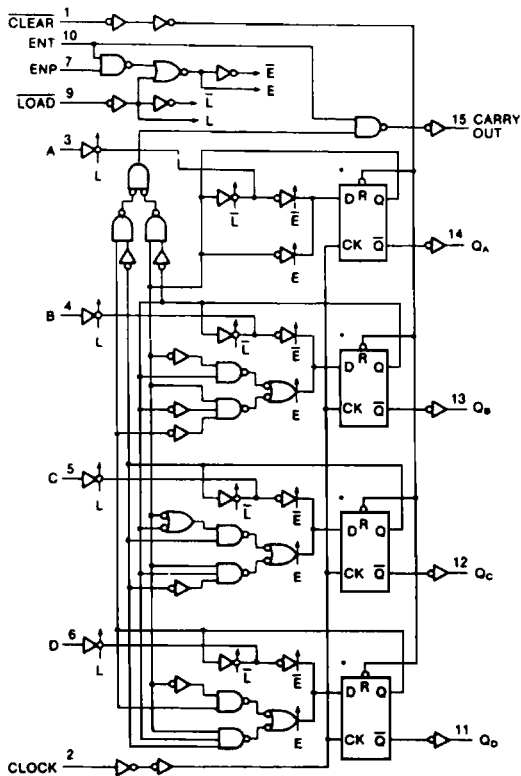
$CARRY = ENT \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D \dots$  (TC74HC161A/163A)



Timing Chart (TC74HC160A/162A: Decade Counter)



Timing Chart (TCHC161A/163A: Binary Counter)

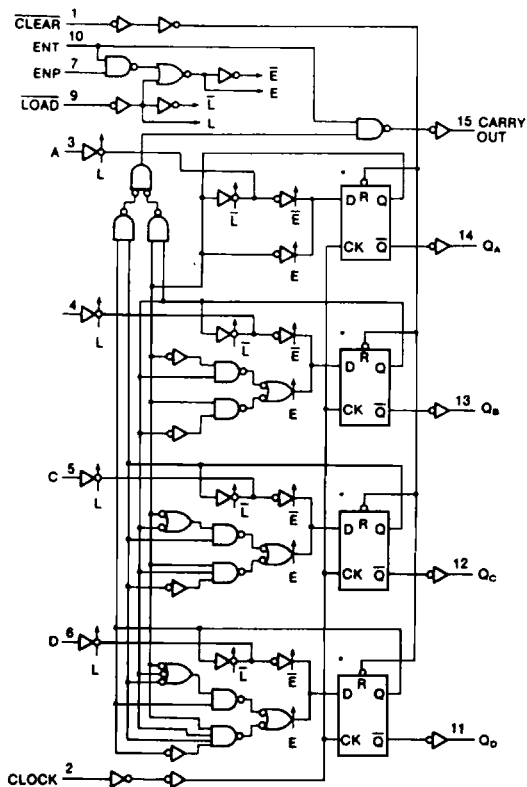


Logic Diagram

Truth Table of Internal F/F

TC74HC160A					TC74HC162A				
D	CK	R	Q	$\bar{Q}$	D	CK	R	Q	$\bar{Q}$
X	X	L	L	H	X	$\bar{\text{L}}$	L	L	H
L	$\bar{\text{L}}$	H	L	H	L	$\bar{\text{L}}$	H	L	H
H	$\bar{\text{L}}$	H	H	L	H	$\bar{\text{L}}$	H	H	L
X	$\bar{\text{L}}$	H	NO CHANGE	L	$\bar{\text{L}}$	H	No Change		

X: Don't Care



Logic Diagram

Truth Table of Internal F/F

TC74HC161A					TC74HC163A				
D	CK	R	Q	$\bar{Q}$	D	CK	R	Q	$\bar{Q}$
X	X	L	L	H	X	$\bar{\text{L}}$	L	L	H
L	$\bar{\text{L}}$	H	L	H	L	$\bar{\text{L}}$	H	L	H
H	$\bar{\text{L}}$	H	H	L	H	$\bar{\text{L}}$	H	H	L
X	$\bar{\text{L}}$	H	NO CHANGE	L	$\bar{\text{L}}$	H	No Change		

X: Don't Care

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Supply Voltage Range	V <sub>CC</sub>	-0.5 ~ 7	V
DC Input Voltage	V <sub>IN</sub>	-0.5 ~ V <sub>CC</sub> + 0.5	V
DC Output Voltage	V <sub>OUT</sub>	-0.5 ~ V <sub>CC</sub> + 0.5	V
Input Diode Current	I <sub>IK</sub>	±20	mA
Output Diode Current	I <sub>OK</sub>	±20	mA
DC Output Current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /Ground Current	I <sub>CC</sub>	±50	mA
Power Dissipation	P <sub>D</sub>	500(DIP)*180(MFP)	mW
Storage Temperature	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temperature 10sec	T <sub>L</sub>	300	°C

\*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

**Recommended Operating Conditions**

Parameter	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	2 ~ 6	V
Input Voltage	V <sub>IN</sub>	0 ~ V <sub>CC</sub>	V
Output Voltage	V <sub>OUT</sub>	0 ~ V <sub>CC</sub>	V
Operating Temperature	T <sub>opr</sub>	-40 ~ 85	°C
Input Rise and Fall Time	t <sub>r</sub> , t <sub>f</sub>	0 ~ 1000(V <sub>CC</sub> = 2.0V) 0 ~ 500(V <sub>CC</sub> = 4.5V) 0 ~ 400(V <sub>CC</sub> = 6.0V)	ns

**DC Electrical Characteristics**

Parameter	Symbol	Test Condition	Ta = 25°C				Ta = -40 ~ 85°C		Unit	
			V <sub>CC</sub>	Min.	Typ.	Max.	Min.	Max.		
High-Level Input Voltage	V <sub>IH</sub>	-	2.0	1.7	-	-	1.7	-	V	
			4.5	3.6	-	-	3.6	-		
			6.0	4.8	-	-	4.8	-		
Low-Level Input Voltage	V <sub>IL</sub>	-	2.0	-	-	0.3	-	0.3	V	
			4.5	-	-	0.9	-	0.9		
			6.0	-	-	1.2	-	1.2		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20μA	2.0	1.8	2.0	-	1.8	-	V
				4.5	4.0	4.5	-	4.0	-	
			I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -5.2mA	4.5	4.18	4.31	-	4.13	-	
				6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20μA	2.0	-	0.0	0.2	-	0.2	V
				4.5	-	0.0	0.5	-	0.5	
			I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 5.2mA	4.5	-	0.17	0.26	-	0.33	
				6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	-	-	±0.1	-	±1.0	μA	
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	-	-	4.0	-	40.0		

Timing Requirements (Input  $t_r = t_f = 6\text{ns}$ )

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 - 85°C	Unit
			V <sub>CC</sub>	Typ.	Limit	Limit	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$	Fig. 1	2.0	–	75	95	ns
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Pulse Width (CLEAR)*	$t_{W(L)}$	Fig. 4	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Setup Time (LOAD, ENP, ENT)	$t_s$	Fig. 4	2.0	–	100	125	
			4.5	–	20	25	
			6.0	–	17	21	
Minimum Setup Time (A, B, C, D)	$t_s$	Fig. 2	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Set-up Time (CLEAR)**	$t_s$	Fig. 5	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Hold Time	$t_h$	Fig 2, 3, 5	2.0	–	0	0	
			4.5	–	0	0	
			6.0	–	0	0	
Minimum Removal Time (CLEAR)*	$t_{rem}$	Fig 4	2.0	–	50	65	
			4.5	–	10	13	
			6.0	–	9	11	
Clock Frequency	f	–	2.0	–	6	5	MHz
			4.5	–	31	25	
			6.0	–	36	29	

AC Electrical Characteristics (C<sub>L</sub> = 15pF, V<sub>CC</sub> = 5V, Ta = 25°C, Input  $t_r = t_f = 6\text{ns}$ )

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	$t_{TLH}$ $t_{THL}$	Fig. 1	–	4	8	ns
Propagation Delay Time (CLOCK-Q)	$t_{PLH}$ $t_{PHL}$	Fig. 1	–	13	21	
Propagation Delay Time (CLOCK-CARRY) (Count Mode)	$t_{PLH}$ $t_{PHL}$	Fig. 1	–	16	26	
Propagation Delay Time (CLOCK-CARRY) (Preset Mode)	$t_{PLH}$	Fig. 2	–	18	30	
	$t_{PHL}$		–	20	35	
Propagation Delay Time (ENT-CARRY)	$t_{PLH}$ $t_{PHL}$	Fig. 6	–	10	17	
Propagation Delay Time (CLEAR-Q)*	$t_{PHL}$	Fig. 4	–	17	26	
Propagation Delay Time (CLEAR-CARRY)*	$t_{PHL}$	Fig. 4	–	20	35	
Maximum Clock Frequency	$f_{MAX}$	–	36	63	–	MHz

\*: for TC74HC160A/161A only

\*\*: for TC74HC162A/163A only

AC Electrical Characteristics (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C		Unit	
			V <sub>CC</sub>	Min.	Typ.	Max.	Min.		Max.
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>	-	2.0	-	25	75	-	95	ns
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Propagation Delay Time (CLOCK-Q)	t <sub>DLH</sub> t <sub>DHL</sub>	Fig. 1	2.0	-	48	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Propagation Delay Time (CLOCK-CARRY) (Count Mode)	t <sub>DLH</sub> t <sub>DHL</sub>	Fig. 1	2.0	-	57	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time (CLOCK-CARRY) (Preset Mode)	t <sub>DLH</sub>	Fig. 2	2.0	-	66	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
	t <sub>DHL</sub>		2.0	-	72	200	-	250	
			4.5	-	24	40	-	50	
			6.0	-	20	34	-	43	
Propagation Delay Time (ENT-CARRY)	t <sub>DLH</sub> t <sub>DHL</sub>	Fig. 6	2.0	-	39	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
Propagation Delay Time (CLEAR-Q)	t <sub>DHL</sub>	Fig. 4	2.0	-	60	150	-	190	
			4.5	-	20	30	-	38	
			6.0	-	17	26	-	33	
Propagation Delay Time (CLEAR-CARRY)	t <sub>DHL</sub>	Fig. 4	2.0	-	72	200	-	250	
			4.5	-	24	40	-	50	
			6.0	-	20	34	-	43	
Maximum Clock Frequency	f <sub>MAX</sub>	-	2.0	6	18	-	5	-	MHz
			4.5	31	53	-	25	-	
			6.0	36	62	-	29	-	
Input Capacitance	C <sub>IN</sub>	-	-	5	10	-	10	pF	
Power Dissipation Capacitance	C <sub>PD(1)</sub>	(1)	-	34	-	-	-		

Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of CPD, and ICC which is obtained from the following formula:

In case of TC74HC160A/162A:

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left( \frac{C_{QA}}{2} + \frac{C_{QB}}{5} + \frac{C_{QC}}{10} + \frac{C_{QD}}{10} + \frac{C_{QD}}{10} \right)$$

In case of TC74HC161A/163A:

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left( \frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{QD}}{16} \right)$$

C<sub>QA</sub> ~ C<sub>QD</sub> and C<sub>CO</sub> are the capacitances at QA ~ QD and CARRY OUT, respectively.

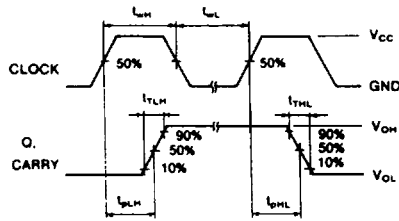
f<sub>CK</sub> is the input frequency of the CLOCK

(2) \* for TC74HC160A/161A only

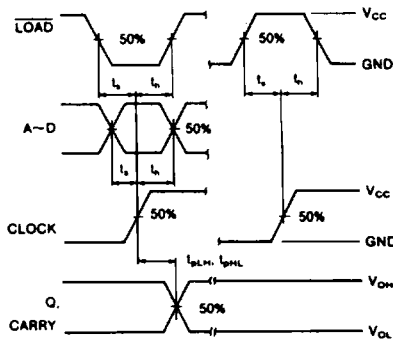
\*\* for TC74HC162/163A only



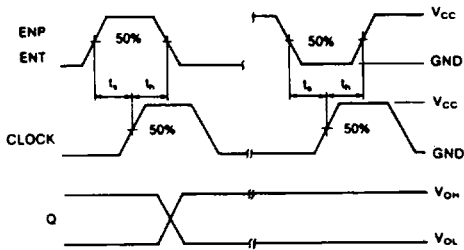
Count Mode (Fig. 1)



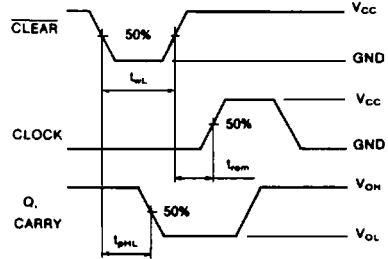
Preset Mode (Fig.2)



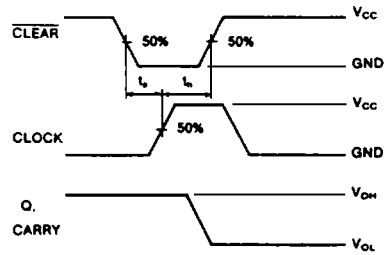
Count Enable Mode (Fig. 3)



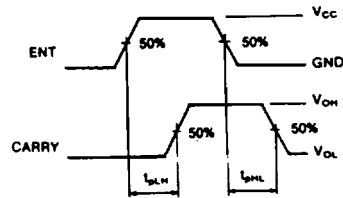
Clear Mode (TC74HC160A/161A) (Fig. 4)



Clear Mode (TC74HC162A/163A) (Fig. 5)

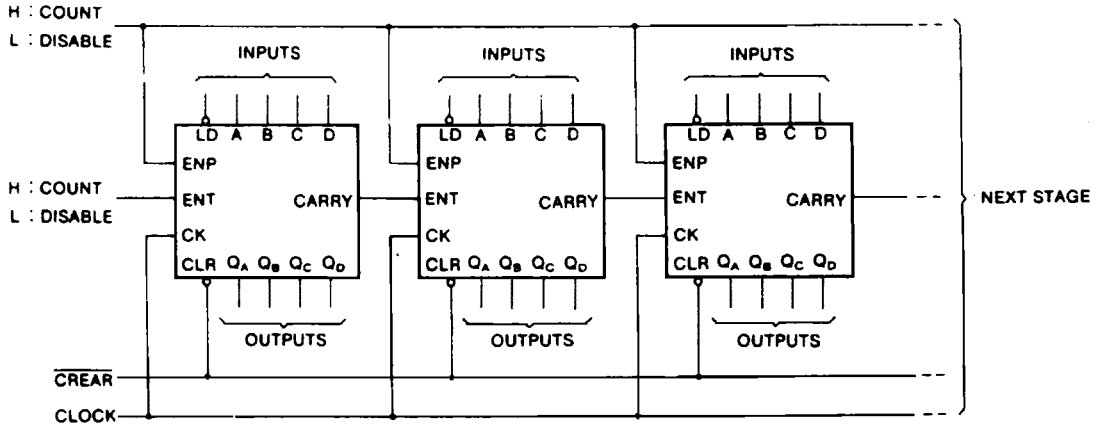


Cascade Mode (Fig. 6)  
(Fix Maximum Count)



Switching Characteristics Test Waveform

PARALLEL CARRY N-BIT COUNTER



Typical Application