# TC74HCT563P
# TC74HCT573P

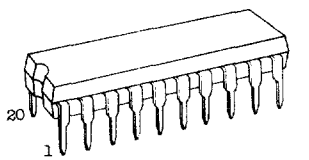
OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT (TTL INPUT LEVEL)

TC74HCT563P INVERTING
TC74HCT573P NON-INVERTING

The TC74HCT563 and TC74HCT573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate $C^2MOS$ technology.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These 8-bit D-type latches are controlled by a latch enable input(LE) and a output enable input($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data.
While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The application designer has a choice of combination of inverting and non-inverting outputs.
The three-state output configuration and the wide choice of outline will make the bus-organized system simple.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

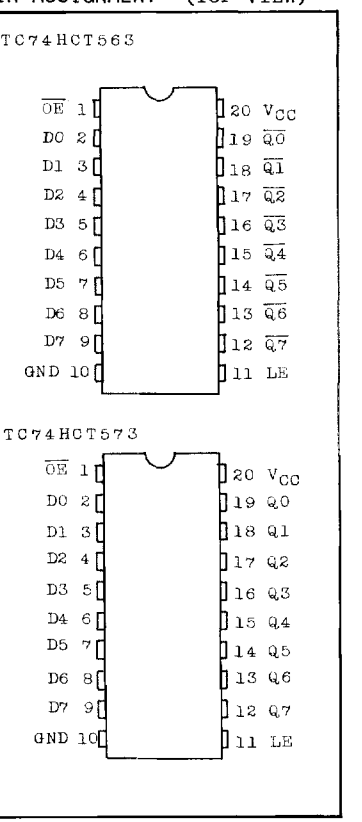
FEATURES:

- High Speed ..... $t_{pd}$=20ns(Typ.)($V_{CC}$=5V)
- Low Power Dissipation ..... $I_{CC}$=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... $V_{IH}$=2V(Min.), $V_{IL}$=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Pin and Function Compatible with 74LS563/573




DIP20(3D20A-P)

PIN ASSIGNMENT (TOP VIEW)



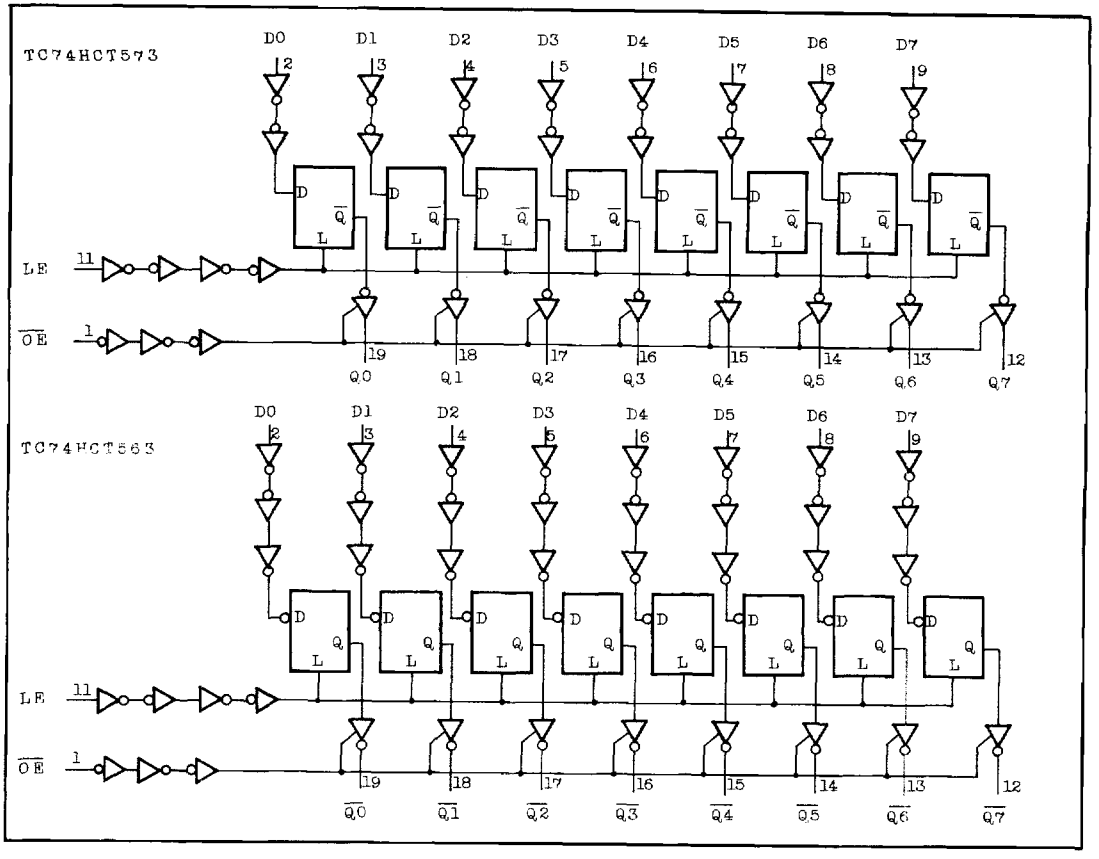

TRUTH TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{OE}$ | LE | D | Q(HCT573) | $\overline{Q}$(HCT563) |
| H | X | X | HZ | HZ |
| L | L | X | Qn | $\overline{Qn}$ |
| L | H | L | L | H |
| L | H | H | H | L |

X : DON'T CARE
HZ : HIGH IMPEDANCE

Qn : Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAM




ABSOLUTE MAXIMUM RATINGS

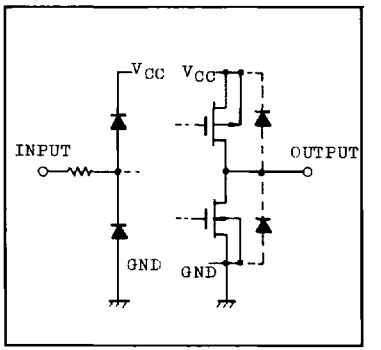
| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | -0.5~7 | V |
| DC Input Voltage | $V_{IN}$ | -0.5~$V_{CC}$+0.5 | V |
| Bus Terminal Voltage | $V_{I/O}$ | -0.5~$V_{CC}$+0.5 | V |
| Input Diode Current | $I_{IK}$ | ±20 | mA |
| Output Diode Current | $I_{OK}$ | ±20 | mA |
| DC Output Current | $I_{OUT}$ | ±35 | mA |
| DC $V_{CC}$/Ground Current | $I_{CC}$ | ±70 | mA |
| Power Dissipation | $P_D$ | 500* | mW |
| Storage Temperature | Tstg | -65~150 | °C |
| Lead Temperature (10 sec) | $T_L$ | 300 | °C |

* 500mW in the range of Ta=-40°C~65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 ∿ 5.5 | V |
| Input Voltage | $V_{IN}$ | 0 ∿ $V_{CC}$ | V |
| Output Voltage | $V_{OUT}$ | 0 ∿ $V_{CC}$ | V |
| Operating Temperature | $T_{opr}$ | −40 ∿ 85 | °C |
| Input Rise and Fall Time | $t_r$, $t_f$ | 0 ∿ 500 ($V_{CC}$=4.5V) | ns |

INPUT and OUTPUT
EQUIVALENT CIRCUIT




DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | | Ta=25°C | | | Ta=−40∿85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ | MIN. | TYP. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage | $V_{IH}$ | | 4.5 ∿ 5.5 | 2.0 | − | − | 2.0 | − | V |
| Low-Level Input Voltage | $V_{IL}$ | | 4.5 ∿ 5.5 | − | − | 0.8 | − | 0.8 | V |
| High-Level Output Voltage | $V_{OH}$ | $V_{IN}$=$V_{IH}$ or $V_{IL}$ | $I_{OH}$=−20μA | 4.5 | 4.4 | 4.5 | − | 4.4 | − | V |
| | | | $I_{OH}$=−6mA | 4.5 | 4.18 | 4.31 | − | 4.13 | − | V |
| Low-Level Output Voltage | $V_{OL}$ | $V_{IN}$=$V_{IH}$ or $V_{IL}$ | $I_{OL}$=20μA | 4.5 | − | 0.0 | 0.1 | − | 0.1 | V |
| | | | $I_{OL}$=6mA | 4.5 | − | 0.17 | 0.26 | − | 0.33 | V |
| 3-State Output Off-State Current | $I_{OZ}$ | $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$V_{OUT}$=$V_{CC}$ or GND | | 5.5 | − | − | ±0.5 | − | ±5.0 | μA |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$=$V_{CC}$ or GND | | 5.5 | − | − | ±0.1 | − | ±1.0 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{IN}$=$V_{CC}$ or GND | | 5.5 | − | − | 4.0 | − | 40.0 | μA |
| | $I_C$ | Per input: $V_{IN}$=2.4V or 0.5V<br>Other input: $V_{CC}$ or GND | | 5.5 | − | − | 2.0 | − | 2.9 | mA |

AC ELECTRICAL CHARACTERISTICS ($C_L$=50pF, Input $t_r=t_f$=6ns)

| PARAMETER | SYMBOL | TEST CONDITION | $V_{CC}$ | Ta=25°C | | | Ta=-40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Output Transition Time | $t_{TLH}$<br>$t_{THL}$ | | 4.5 | - | 7 | 12 | - | 19 | ns |
| Propagation Delay Time (LE - Q, $\overline{Q}$) | $t_{pLH}$<br>$t_{pHL}$ | | 4.5 | - | 24 | 35 | - | 44 | |
| Propagation Delay Time (D - Q, $\overline{Q}$) | $t_{pLH}$<br>$t_{pHL}$ | | 4.5 | - | 22 | 35 | - | 44 | |
| Minimum Pulse Width (LE) | $t_{w(H)}$ | | 4.5 | - | 8 | 15 | - | 19 | |
| Minimum Set-up Time | $t_s$ | | 4.5 | - | 2 | 10 | - | 13 | |
| Minimum Hold Time | $t_h$ | | 4.5 | - | - | 5 | - | 5 | |
| 3-State Output Enable Time | $t_{pZL}$<br>$t_{pZH}$ | $R_L$=1kΩ | 4.5 | - | 18 | 35 | - | 44 | |
| 3-State Output Disable Time | $t_{pLZ}$<br>$t_{pHZ}$ | $R_L$=1kΩ | 4.5 | - | 26 | 37 | - | 46 | |
| Input Capacitance | $C_{IN}$ | | | - | 5 | 10 | - | 10 | pF |
| Output Capacitance | $C_{OUT}$ | | | - | 10 | - | - | - | |
| Power Dissipation Capacitance | $C_{PD}$(1) | TC74HCT563 | | - | 41 | - | - | - | |
| | | TC74HCT573 | | - | 41 | - | - | - | |

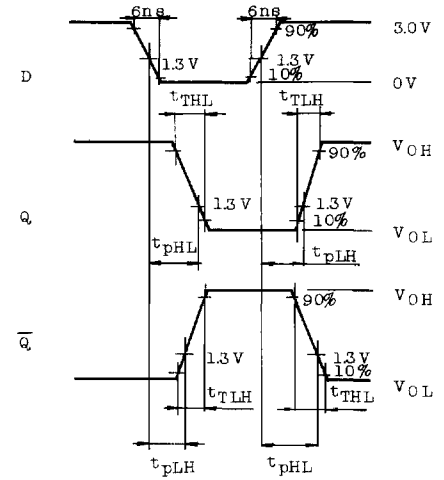
Note (1): $C_{PD}$ is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

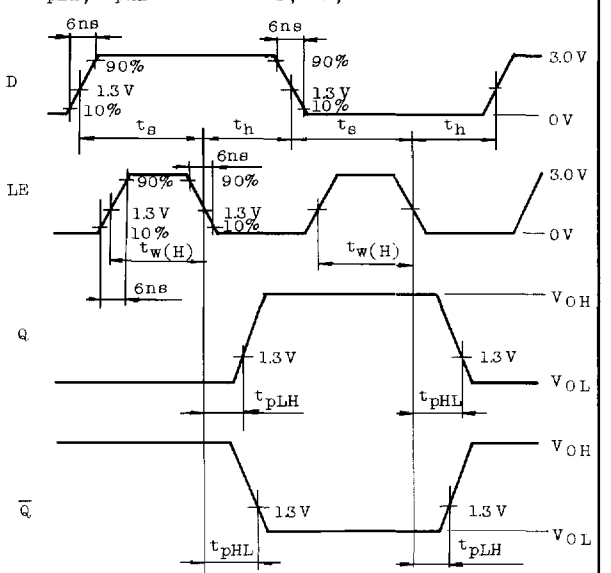
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Latch)}$$

## SWITCHING CHARACTERISTICS TEST WAVEFORM

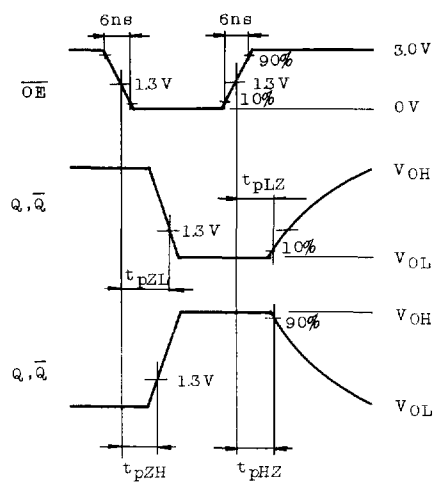
$t_{TLH}$, $t_{THL}$, $t_{pLH}$, $t_{pHL}$

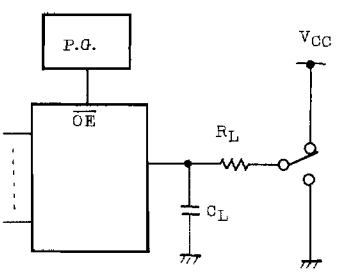



$t_{pLH}$, $t_{pHL}$(LE-Q,$\overline{Q}$), $t_s$, $t_h$, $t_w$




$t_{pLZ}$, $t_{pHZ}$, $t_{pZL}$, $t_{pZH}$




(NOTE)
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO $V_{CC}$ LINE.

$I_{CC}$(Opr.) TEST CIRCUIT