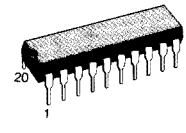
SGS-THOMSON MICROELECTRONICS

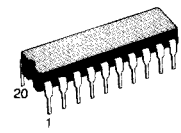
M54HCT245/640/643
M74HCT245/640/643

OCTAL BUS TRANSCEIVER (3-STATE)
HCT245 NON INVERTING, HCT640 INVERTING, HCT643 INVERTING/NON INVERTING

- LOW POWER DISSIPATION
  $I_{CC} = 4\mu A$ (MAX.) at $T_A = 25°C$
- COMPATIBLE WITH TTL OUTPUTS
  $V_{IH} = 2V$ (MIN) $V_{IL} = 0.8V$ (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ $I_{OL} = 6mA$ (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS245/640/643



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCTXXX F1
M74HCTXXX B1N
M74HCTXXX F1
M74HCTXXX C1
M74HCTXXX M1

DESCRIPTION

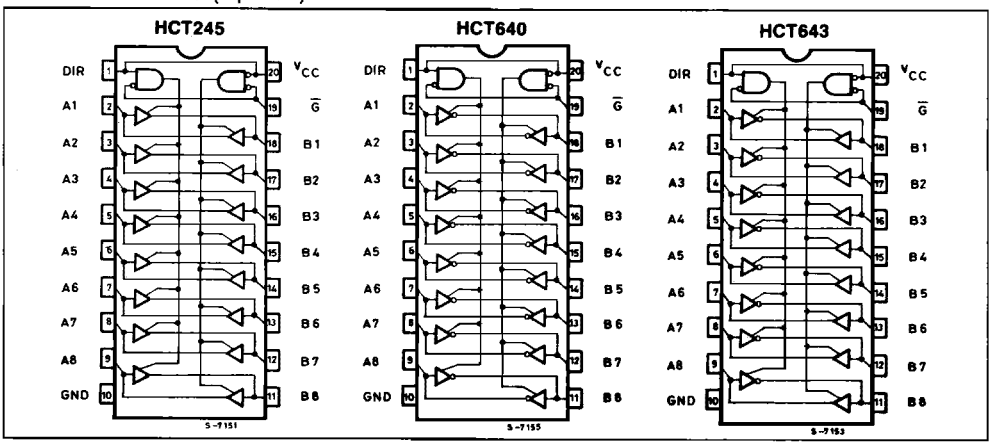
The HCT245, HCT640, and HCT643 utilize silicon gate C²MOS technology to achieve operating speeds equivalent to LSTTL parts.
Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it possesses the capability to drive of 15 LSTTL loads. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

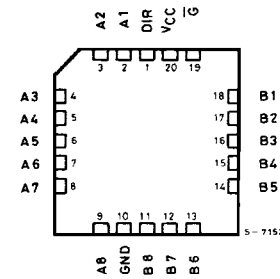
NOTICE FOR APPLICATION

IT IS NOT POSSIBLE TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN THE OUTPUT MODE. PULL UP OR PULL DOWN RESISTOR SHOULD BE USED ON HIGH IMPEDANCE (3-STATE) FLOATING BUS TERMINAL

PIN CONNECTIONS (top view)

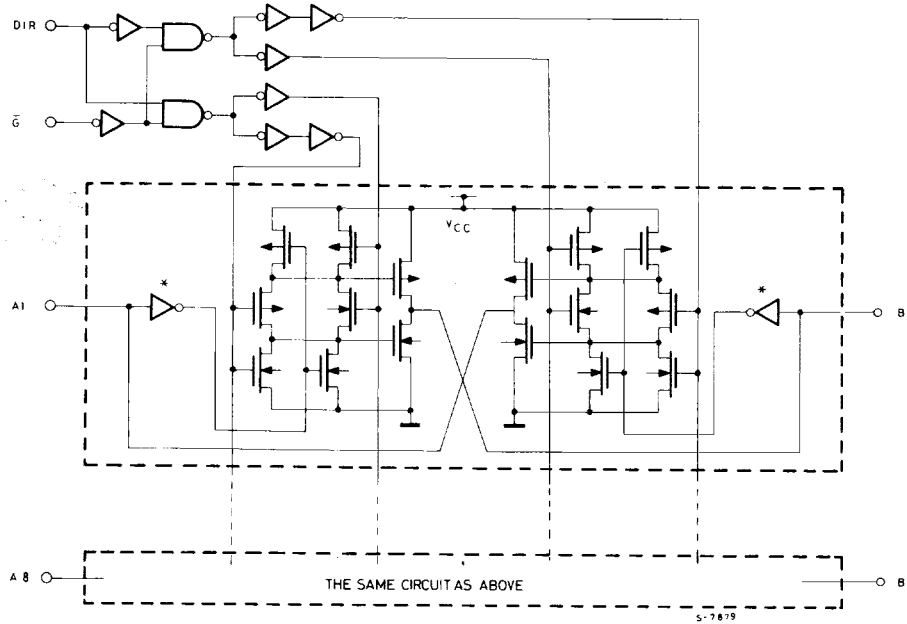


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM (HCT 640)



NOTE: IN CASE OF HCT245 OR HCT643, INPUT INVERTERS MARKED * AT A BUS OR AT B BUS ARE ELIMINATED RESPECTIVELY.

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HCT245	HCT640	HCT643
L	L	OUTPUT	INPUT	A=B	A=B	A=B
L	H	INPUT	OUTPUT	B=A	B=A	B=A
H	X	Z	Z	Z	Z	Z

X: DON'T CARE
Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 6.0			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								
			V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	V
				−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Output Off-State Current	5.5	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10.0	
I_{IN}	Input Leakage Current	5.5	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: $V_{IN} = 0.5V$ or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	8	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5		—	19	28	—	35	—	42	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	4.5	$R_L = 1k\Omega$	—	27	42	—	53	—	63	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	4.5	$R_L = 1k\Omega$	—	27	40	—	50	—	60	ns

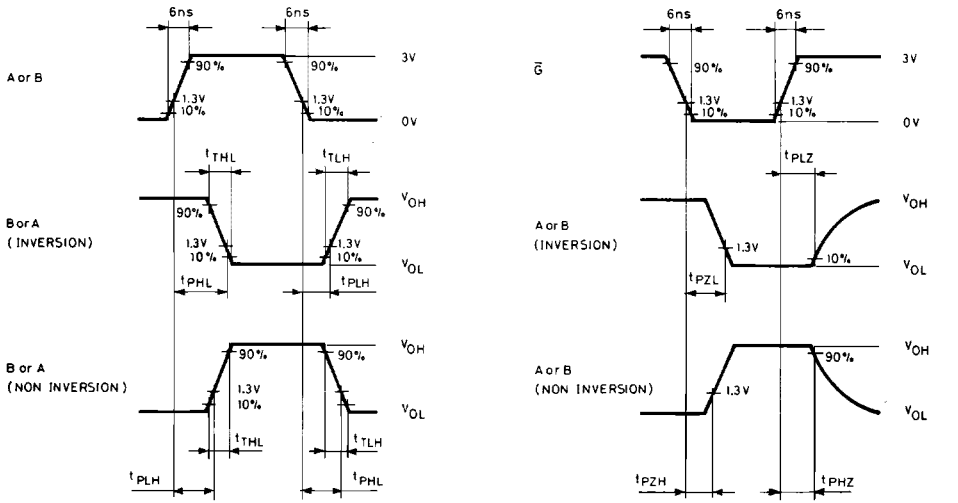
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance		DIR, G, $\overline{G}$,	—	5	10	—	10	—	10	pF
$C_{I/O}$	Bus Inp. Capacit.		An, Bn	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HCT245	—	46	—	—	—	—	—	pF
			M54/74HCT640/643	—	44	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).

Average operating current can be obtained by the following equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate)

SWITCHING CHARACTERISTICS TEST WAVEFORM



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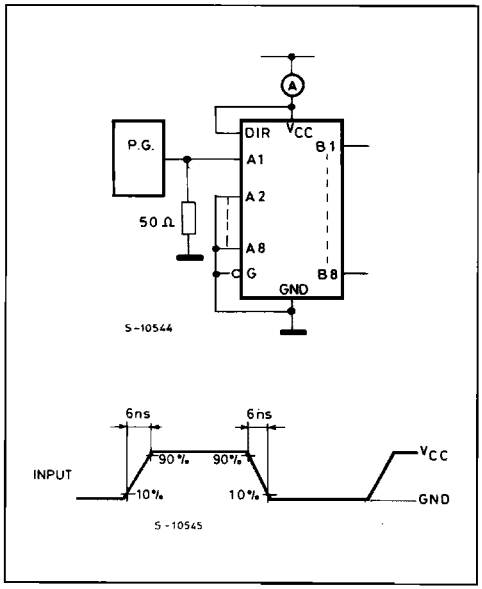
TEST CIRCUIT



C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite

$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$

In determining the typical value of C_{PD}, a relatively high frequency of 1MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current