M74HC160P

PRESETTABLE BCD COUNTER WITH ASYNCHRONOUS RESET

DESCRIPTION

The M74HC160 is a semiconductor integrated circuit consisting of a presettable synchronous BCD counter with direct reset input.

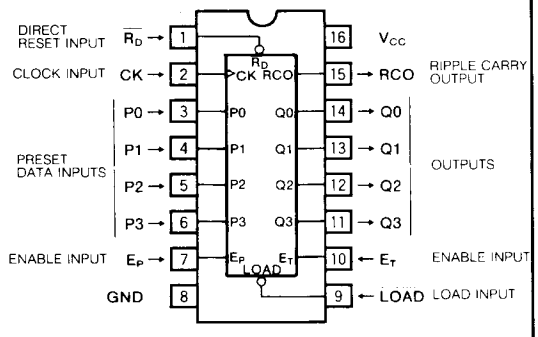
FEATURES

- Direct reset and synchronous preset inputs
- Enable input and ripple carry output for cascade connection
- High-speed: (clock frequency) 45MHz typ. (C_L=15pF, V_{CC}=5V)
- Low power dissipation: 20μW/package (max) (V_{CC}=5V, T_a=25℃, quiescent state)
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



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FUNCTIONAL DESCRIPTION

When the count pulse is applied to clock input CK, the number of count pulses will be output at outputs Q0 through Q3 synchronous with the count pulse in BCD code. Counting takes place when CK changes from low-level to high-level.

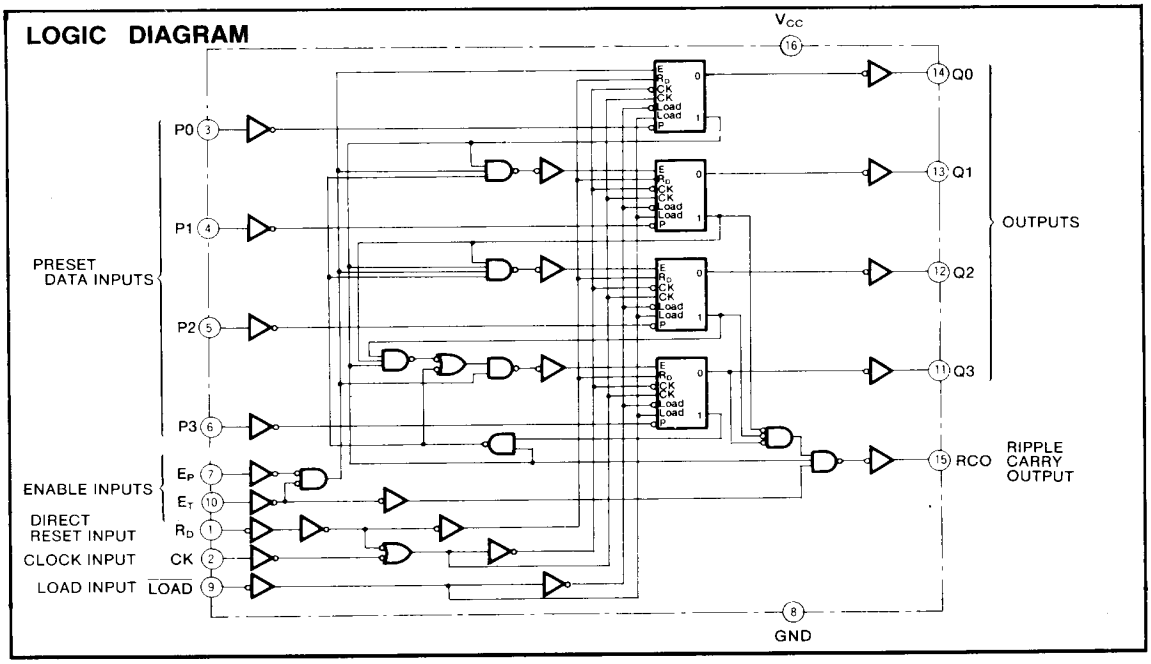
The preset functions synchronously with the count pulse. By supplying data to preset data inputs P0 through P3 and setting load input $\overline{LOAD}$ to low-level, when CK changes from low-level to high-level, the P0 through P3 signals will be output to Q0 through Q3, respectively, irrespective of enable inputs E_P and E_T. This permits presetting of the counter.

When values greater than 10 are preset, the count advances as shown in the State Transition Diagram.

The reset operates asynchronously, and by setting direct reset input $\overline{R_D}$ to low-level, Q0 through Q3 will become low irrespective of other inputs.

The ripple carry output RCO will become high only when Q0 is high, Q1 is low, Q2 is low, Q3 is high, and E_T is high. E_P, E_T and RCO are used in cascade connections of the counter in synchronous form when the counter is set up in a 10n arrangement. (See the Application Example.)

LOGIC DIAGRAM



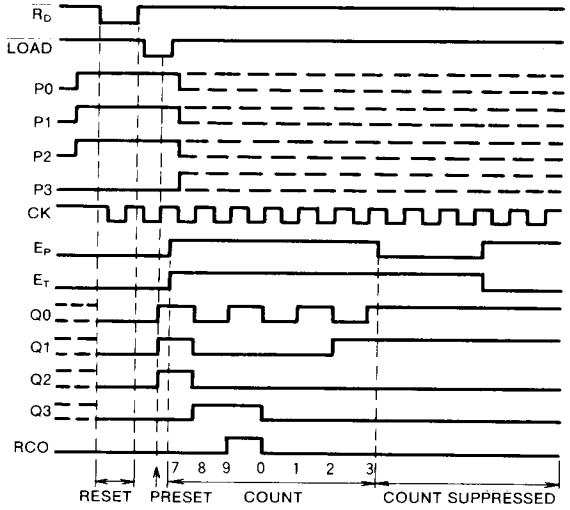
PRESETTABLE BCD COUNTER WITH ASYNCHRONOUS RESET

FUNCTION TABLE (Note 1)

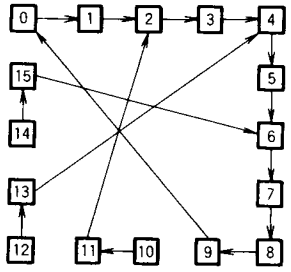
Inputs					Outputs				
$\overline{R_D}$	LOAD	E_T	E_P	CK	Q0	Q1	Q2	Q3	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	P0	P1	P2	P3	L
H	L	H	X	↑	P0	P1	P2	P3	L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Count suppressed				L
H	H	H	L	X	Count suppressed				L*

Note 1 : ↑ : Change from low to high level
* : RCO is normally low, but becomes high when Q0 is high, Q1 is low, Q2 is low, Q3 is high, and E_T is high. Accordingly, RCO=Q0 · $\overline{Q1}$ · $\overline{Q2}$ · Q3 · E_T
: X : Irrelevant

OPERATION TIMING DIAGRAM



STATE TRANSITION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current, per output pin		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation		500	mW
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

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ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃		−40～+85℃		
				V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V I_O = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V I_O = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −4.0mA	4.5	4.18			4.13		
			I_{OH} = −5.2mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 4.0mA	4.5			0.26		0.33	
			I_{OL} = 5.2mA	6.0			0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

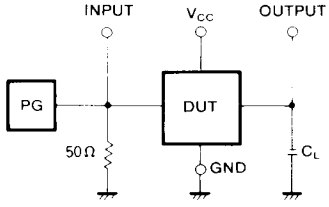
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 3)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level				10	ns
t_{THL}	output transition time				10	
t_{PLH}	Low-level to high-level and high-level to low-level				28	ns
t_{PHL}	output propagation time (CK −Q)				34	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)				36	ns
t_{PLH}	Low-level to high-level and high-level to low-level				26	ns
t_{PHL}	output propagation time (E_T − RCO)				32	
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (CK − RCO)				36	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)				38	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits						Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency		2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t_{THL}			2.0			75		95	
			4.5			15		19	
			6.0			13		16	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			205		258	
			4.5			41		52	
			6.0			35		44	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − Q)	C_L = 50pF (Note 3)	2.0			210		265	ns
			4.5			42		53	
			6.0			36		45	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (E_T − RCO)		2.0			160		202	ns
			4.5			32		40	
			6.0			27		34	
t_{PHL}			2.0			195		246	
			4.5			39		49	
			6.0			33		42	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − RCO)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			215		271	
			4.5			43		54	
			6.0			37		46	
t_{PHL}	High-level to low-level output propagation time ($\overline{R_D}$ − RCO)		2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
C_I	Input capacitance					10		10	pF
C_{PD}	Power dissipation capacitance (Note 2)				57				pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit

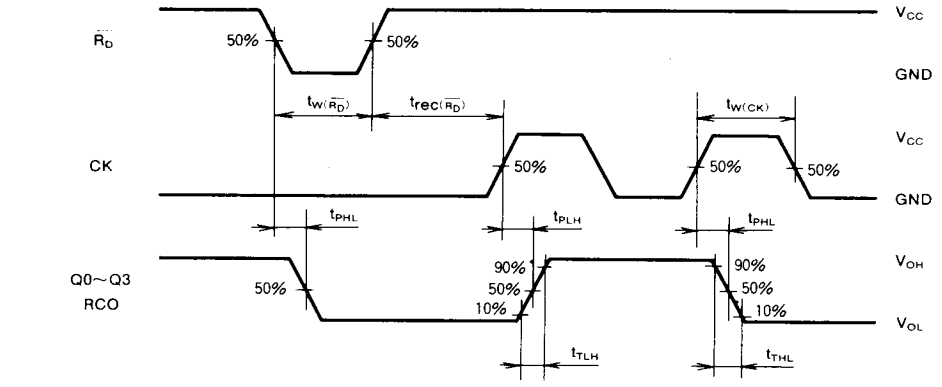


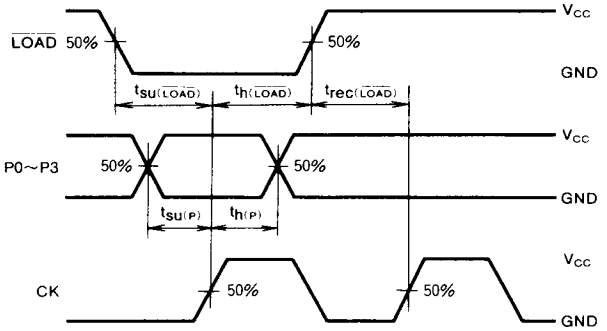
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

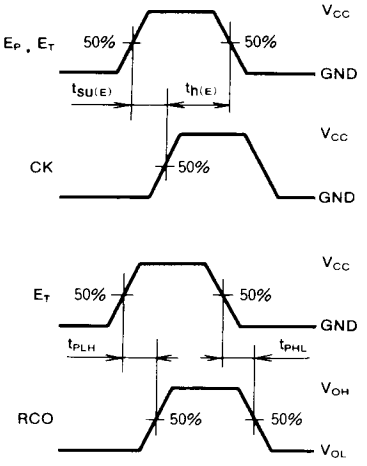
TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
				25℃		−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
$t_{w(CK)}$	Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{w(\overline{R_D})}$	Direct reset pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
$t_{su(P)}$	P setup time with respect to CK		2.0	150			189		ns
			4.5	30			38		
			6.0	26			32		
$t_{su(\overline{LOAD})}$	$\overline{LOAD}$ setup time with respect to CK		2.0	135			170		ns
			4.5	27			34		
			6.0	23			29		
$t_{su(E)}$	E_T, E_P setup time with respect to CK		2.0	200			250		ns
			4.5	40			50		
			6.0	34			43		
$t_{h(P)}$	P hold time with respect to CK		2.0	50			63		ns
			4.5	10			13		
			6.0	9			11		
$t_{h(\overline{LOAD})}$	$\overline{LOAD}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{h(E)}$	E_T, E_P hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
$t_{rec(\overline{R_D})}$	$\overline{R_D}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		
$t_{rec(LOAD)}$	$\overline{LOAD}$ recovery time with respect to CK		2.0	125			158		ns
			4.5	25			32		
			6.0	21			27		

TIMING DIAGRAM



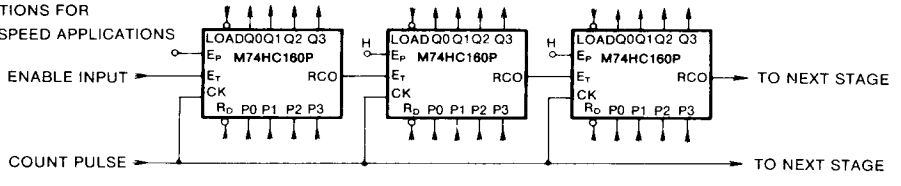




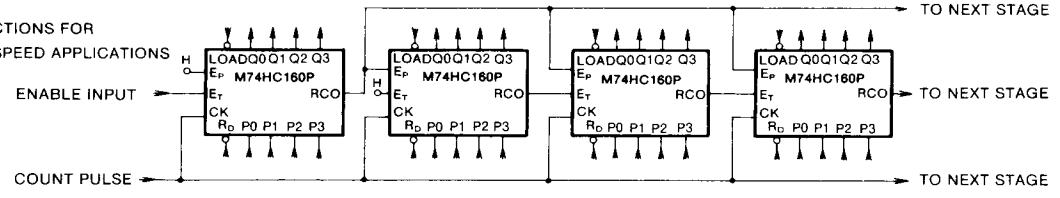
APPLICATION EXAMPLE

10^n COUNTER USING CASCADE CONNECTION

● CONNECTIONS FOR LOW-SPEED APPLICATIONS



● CONNECTIONS FOR HIGH-SPEED APPLICATIONS



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