

# MC14528B

## Dual Monostable Multivibrator

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components,  $C_X$  and  $R_X$ .

### Features

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- This part should only be used in new designs where the pulse width is  $< 10 \mu\text{s}$   
 Note: For designs requiring a pulse width  $> 10 \mu\text{s}$ , please see MC14538, which is pin-for-pin compatible
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Rating	Symbol	Value	Unit
DC Supply Voltage Range	$V_{DD}$	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	$V_{in}, V_{out}$	-0.5 to $V_{DD} + 0.5$	V
Input or Output Current (DC or Transient) per Pin	$I_{in}, I_{out}$	$\pm 10$	mA
Power Dissipation, per Package (Note 1)	$P_D$	500	mW
Ambient Temperature Range	$T_A$	-55 to +125	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}\text{C}$
Lead Temperature (8-Second Soldering)	$T_L$	260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### 1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

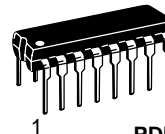
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



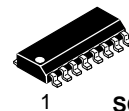
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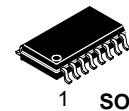
### MARKING DIAGRAMS



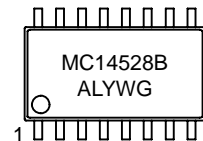
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



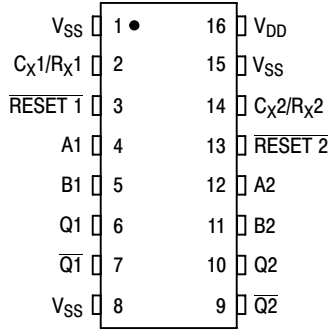
- A = Assembly Location
- WL = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G = Pb-Free Package

### ORDERING INFORMATION

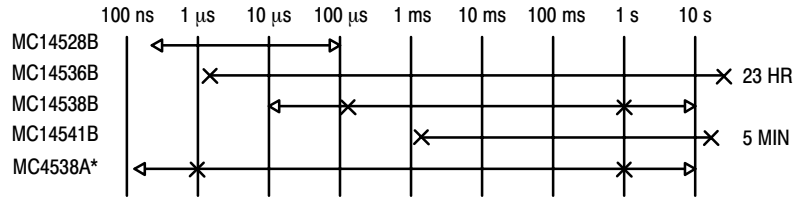
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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## PIN ASSIGNMENT



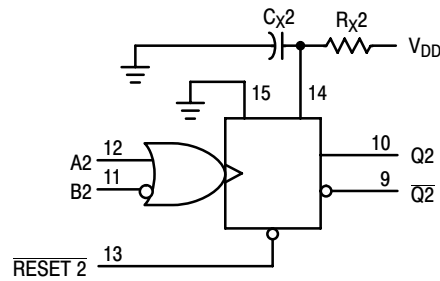
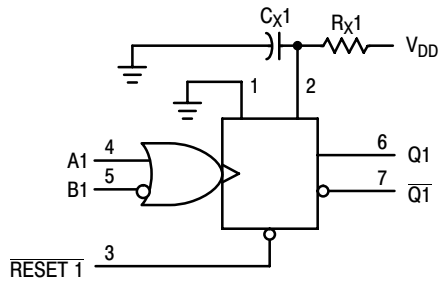
## ONE-SHOT SELECTION GUIDE



\*LIMITED OPERATING VOLTAGE (2-6 V)

TOTAL OUTPUT PULSE WIDTH RANGE  $\longleftrightarrow$   
 RECOMMENDED PULSE WIDTH RANGE  $\times \longleftrightarrow \times$

## BLOCK DIAGRAM



$V_{DD}$  = PIN 16  
 $V_{SS}$  = PIN 1, PIN 8, PIN 15  
 $R_x$  AND  $C_x$  ARE EXTERNAL COMPONENTS

## FUNCTION TABLE

Reset	Inputs		Outputs	
	A	B	Q	Q̄
H		H		
H	L			
H		L	Not Triggered	Not Triggered
H	H		Not Triggered	Not Triggered
H	L, H,	H	Not Triggered	Not Triggered
H	L	L, H,	Not Triggered	Not Triggered
L	X	X	L	H
	X	X	Not Triggered	Not Triggered

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage "0" Level V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
15		-	0.05	-	0	0.05	-	0.05			
"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc	
		10	9.95	-	9.95	10	-	9.95	-		
		15	14.95	-	14.95	15	-	14.95	-		
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
15		-	4.0	-	6.75	4.0	-	4.0			
"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc	
		10	7.0	-	7.0	5.50	-	7.0	-		
		15	11	-	11	8.25	-	11	-		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source    Sink	I <sub>OH</sub>	5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	mAdc
			5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
10			-1.6	-	-1.3	-2.25	-	-0.9	-		
15			-4.2	-	-3.4	-8.8	-	-2.4	-		
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OL</sub>	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc	
		10	1.6	-	1.3	2.25	-	0.9	-		
		15	4.2	-	3.4	8.8	-	2.4	-		
Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	-	5.0	-	0.005	5.0	-	150	μAdc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Total Supply Current at an external load Capacitance (C <sub>L</sub> ) and at external timing capacitance (C <sub>X</sub> ), use the formula. (Note 3)	I <sub>T</sub>	-	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2 \times 10^{-8} R_X C_X (V_{DD}^{-2})^2 f] \times 10^{-3}$ where: I <sub>T</sub> in μA (per circuit), C <sub>L</sub> and C <sub>X</sub> in pF, R <sub>X</sub> in megohms, V <sub>DD</sub> in Vdc, f in kHz is input frequency.							μAdc	

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

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## SWITCHING CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ ) (Note 4)

Characteristic	Symbol	$C_X$ pF	$R_X$ k $\Omega$	$V_{DD}$ Vdc	Min	Typ (Note 5)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	–	–	5.0 10 15	– – –	100 50 40	200 100 80	ns
Turn-Off, Turn-On Delay Time — A or B to Q or $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 240 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	15	5.0	5.0 10 15	– – –	325 120 90	650 240 180	ns
Turn-Off, Turn-On Delay Time — A or B to Q or $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	1000	10	5.0 10 15	– – –	705 290 210	– – –	ns
Input Pulse Width — A or B	$t_{WH}$	15	5.0	5.0	150	70	–	ns
				10	75	30	–	ns
	$t_{WL}$	1000	10	5.0	–	70	–	ns
				10	–	30	–	ns
15	–	30	–	ns				
Output Pulse Width — Q or $\bar{Q}$ (For $C_X < 0.01 \mu\text{F}$ use graph for appropriate $V_{DD}$ level.)	$t_W$	15	5.0	5.0 10 15	– – –	550 350 300	– – –	ns
Output Pulse Width — Q or $\bar{Q}$ (For $C_X > 0.01 \mu\text{F}$ use formula: $t_W = 0.2 R_X C_X \ln [V_{DD} - V_{SS}]$ ) (Note 6)	$t_W$	10,000	10	5.0 10 15	15 10 15	30 50 55	45 90 95	$\mu\text{s}$
Pulse Width Match between Circuits in the same package	$t_1 - t_2$	10,000	10	5.0 10 15	– – –	6.0 8.0 8.0	25 35 35	%
Reset Propagation Delay — $\bar{\text{Reset}}$ to Q or $\bar{Q}$	$t_{PLH}$ , $t_{PHL}$	15	5.0	5.0	–	325	600	ns
				10	–	90	225	ns
		1000	10	5.0	–	1000	–	ns
				10	–	300	–	ns
15	–	250	–	ns				
Retrigger Time	$t_{rr}$	15	5.0	5.0	0	–	–	ns
				10	0	–	–	ns
15	0	–	–	ns				
1000	10	5.0	0	–	–	ns		
10	0	–	–	ns				
15	0	–	–	ns				
External Timing Resistance	$R_X$	–	–	–	5.0	–	1000	k $\Omega$
External Timing Capacitance	$C_X$	–	–	–	No Limits (Note 7)			$\mu\text{F}$

4. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6. If  $C_X > 15 \mu\text{F}$ , Use Discharge Protection Diode  $D_X$ , per Figure 9.

7.  $R_X$  is in  $\Omega$ ,  $C_X$  is in farads,  $V_{DD}$  and  $V_{SS}$  in volts,  $PW_{out}$  in seconds.

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## ORDERING INFORMATION

Device	Package	Shipping†
MC14528BCP	PDIP-16	25 Units / Rail
MC14528BCPG	PDIP-16 (Pb-Free)	
MC14528BD	SOIC-16	48 Units / Rail
MC14528BDG	SOIC-16 (Pb-Free)	
MC14528BDR2	SOIC-16	2500 / Tape & Reel
MC14528BDR2G	SOIC-16 (Pb-Free)	
MC14528BF	SOEIAJ-16	50 Units / Rail
MC14528BFG	SOEIAJ-16 (Pb-Free)	
MC14528BFEL	SOEIAJ-16	2000 / Tape & Reel
MC14528BFELG	SOEIAJ-16 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

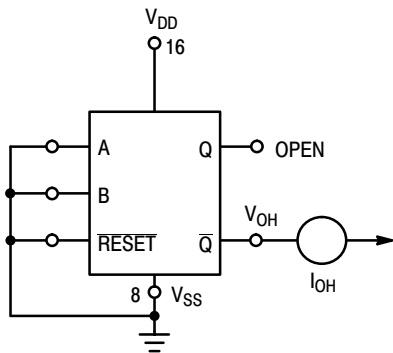


Figure 1. Output Source Current Test Circuit

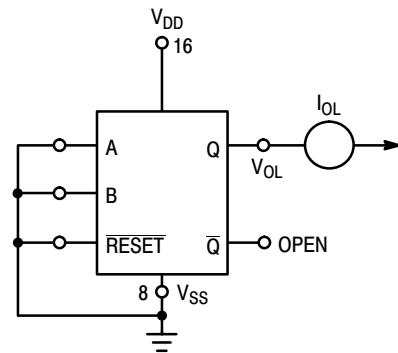


Figure 2. Output Sink Current Test Circuit

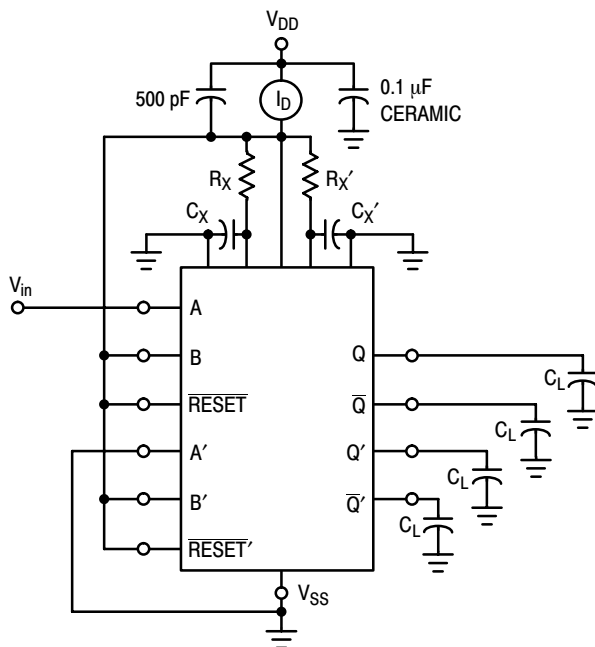
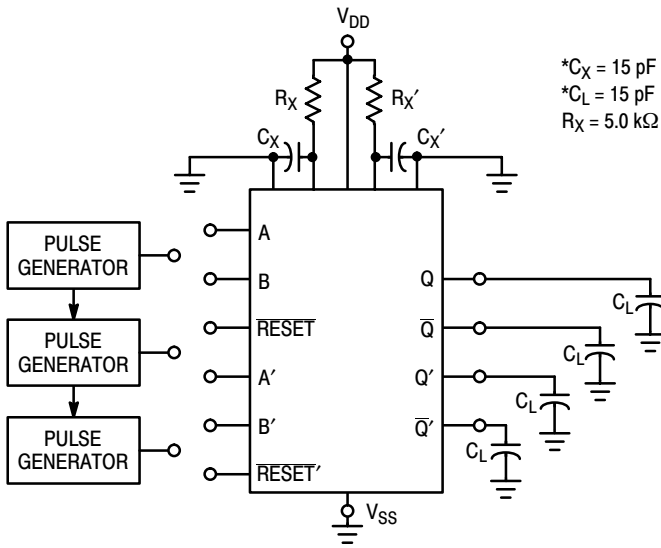


Figure 3. Power Dissipation Test Circuit and Waveforms

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## INPUT CONNECTIONS

Characteristics	Reset	A	B
$t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, t_W$	$V_{DD}$	PG1	$V_{DD}$
$t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, t_W$	$V_{DD}$	$V_{SS}$	PG2
$t_{PLH(R)}, t_{PHL(R)}, t_W$	PG3	PG1	PG2

\*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

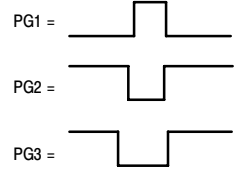


Figure 4. AC Test Circuit

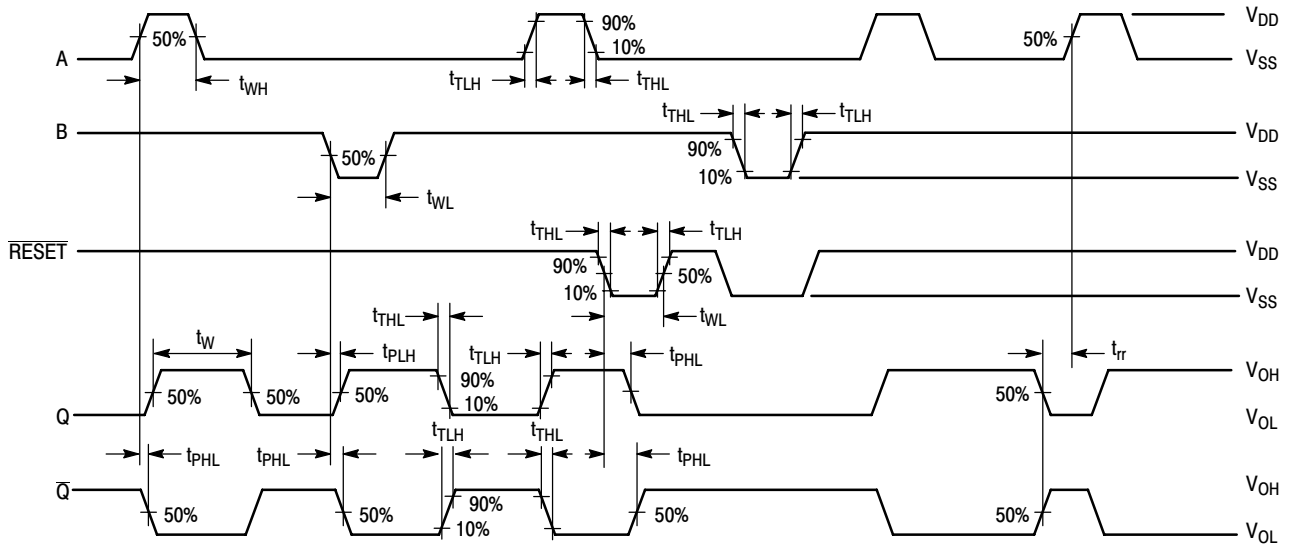


Figure 5. AC Test Waveforms

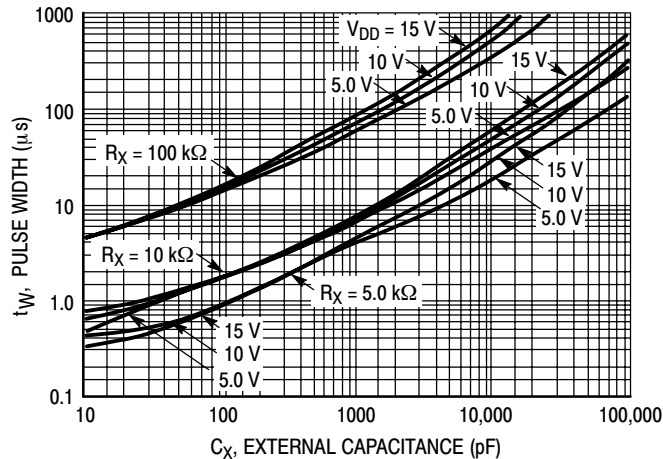
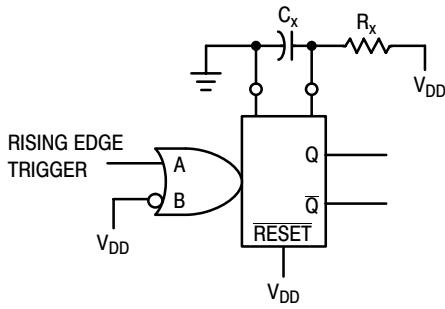


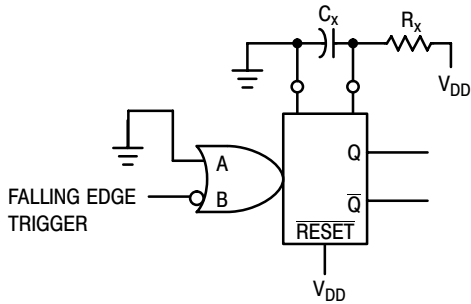
Figure 6. Pulse Width versus  $C_X$

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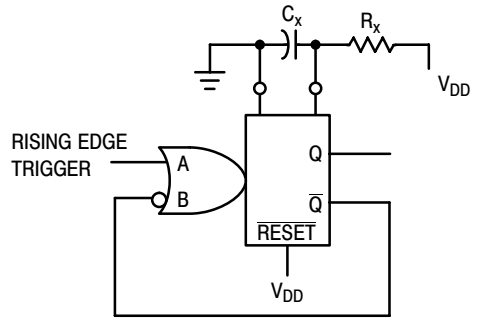
## TYPICAL APPLICATIONS



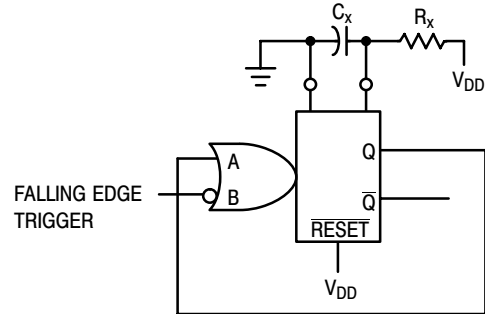
**Figure 7. Retriggerable Monostables Circuitry**



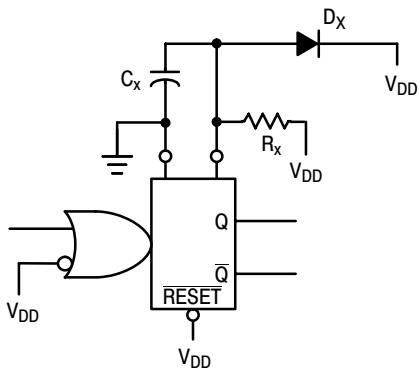
**Figure 7. Retriggerable Monostables Circuitry**



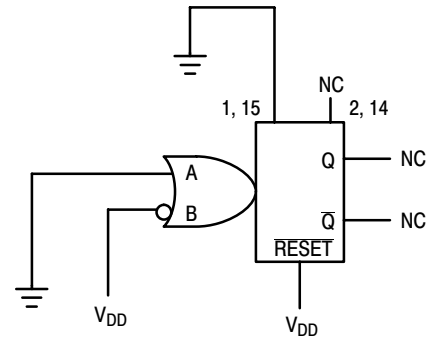
**Figure 8. Non-Retriggerable Monostables Circuitry**



**Figure 8. Non-Retriggerable Monostables Circuitry**



**Figure 9. Use of a Diode to Limit Power Down Current Surge**

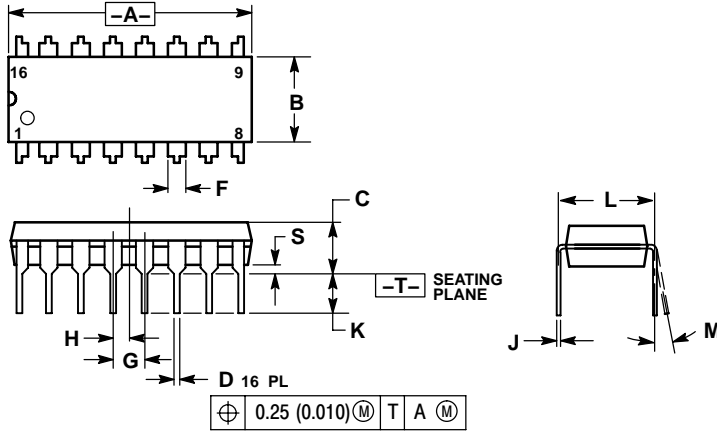


**Figure 10. Connection of Unused Sections**

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## PACKAGE DIMENSIONS

PDIP-16  
CASE 648-08  
ISSUE T

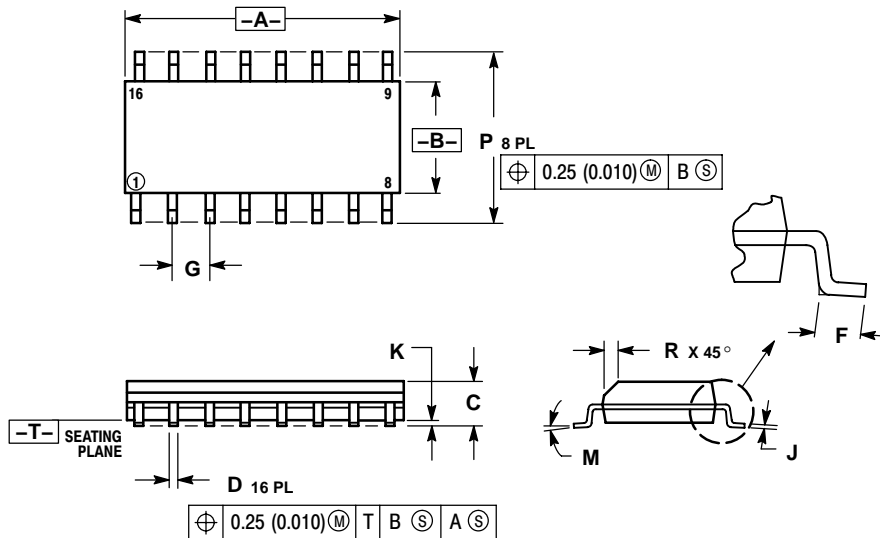


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16  
CASE 751B-05  
ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

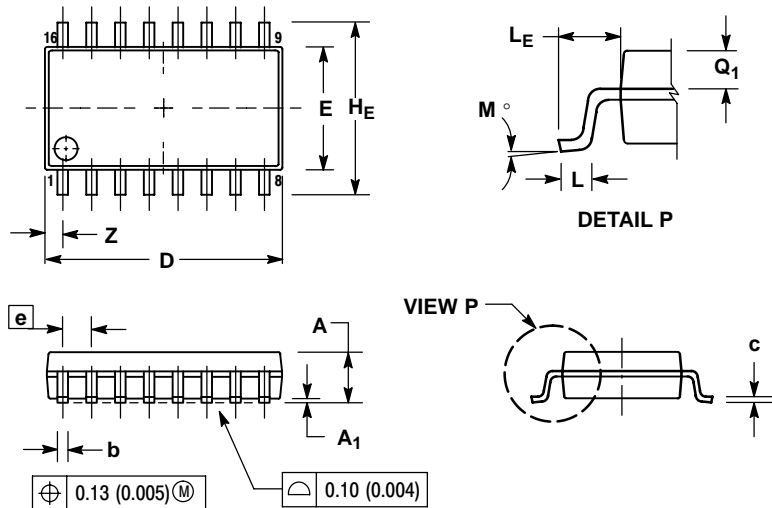
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019



# MC14528B

## PACKAGE DIMENSIONS

SOEIAJ-16  
CASE 966-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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