

**QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE****DESCRIPTION**

The M74HC266 is a semiconductor integrated circuit consisting of four 2-input exclusive NOR gates.

**FEATURES**

- High-speed: 9ns typ. ( $C_L=15\text{pF}$ ,  $V_{CC}=5\text{V}$ )
- Low power dissipation:  $5\mu\text{W}/\text{package (max)}$  ( $V_{CC}=5\text{V}$ ,  $T_a=25^\circ\text{C}$ , quiescent state)
- High noise margin: 30% of  $V_{CC}$ , min. ( $V_{CC}=4.5\text{V}, 6\text{V}$ )
- Capable of driving 10 LSTTL loads
- Wide operating voltage range:  $V_{CC}=2\sim6\text{V}$
- Wide operating temperature range:  $T_a=-40\sim85^\circ\text{C}$

**APPLICATION**

General purpose, for use in industrial and consumer digital equipment.

**FUNCTIONAL DESCRIPTION**

Use of silicon gate technology allows the M74HC266 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS266.

Buffered outputs Y improve input-to-output transfer characteristics and reduce to a minimum output impedance variations with respect to input voltage variations.

When both inputs A and B are either high or low, the output Y will become high, and when the levels of A and B are opposite, the output Y will become low.

Note that the output of M74HC266 and 74LS266 differ in that the output of the M74HC266 is not open drain.

**FUNCTION TABLE**

Inputs		Output
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	H

**ABSOLUTE MAXIMUM RATINGS** ( $T_a = -40\sim+85^\circ\text{C}$ )

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		$-0.5\sim+7.0$	V
$V_i$	Input voltage		$-0.5\sim V_{CC}+0.5$	V
$V_o$	Output voltage		$-0.5\sim V_{CC}+0.5$	V
$I_{IK}$	Input protection diode current	$V_i < 0\text{V}$	-20	mA
		$V_i > V_{CC}$	20	
$I_{OK}$	Output parasitic diode current	$V_o < 0\text{V}$	-20	mA
		$V_o > V_{CC}$	20	
$I_o$	Output current, per output pin		$\pm 25$	mA
$I_{CC}$	Supply/GND current	$V_{CC}, \text{GND}$	$\pm 50$	mA
$P_d$	Power dissipation		500	mW
$T_{stg}$	Storage temperature range		-65~+150	°C



QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

RECOMMENDED OPERATING CONDITIONS ( $T_a = -40 \sim +85^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{CC}$	Supply voltage	2		6	V
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$T_{opr}$	Operating temperature range	-40		+85	$^\circ\text{C}$
$t_r, t_f$	Input risetime, falltime	$V_{CC} = 2.0\text{V}$	0	1000	ns
		$V_{CC} = 4.5\text{V}$	0	500	
		$V_{CC} = 6.0\text{V}$	0	400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits					Unit
			$V_{CC}(\text{V})$	Min	Typ	Max	Min	
$V_{IH}$	High-level input voltage	$V_O = 0.1\text{V}, V_{CC} = 0.1\text{V}$ $I_O = 20\mu\text{A}$	2.0	1.5			1.5	V
			4.5	3.15			3.15	
			6.0	4.2			4.2	
$V_{IL}$	Low-level input voltage	$V_O = 0.1\text{V}, V_{CC} = 0.1\text{V}$ $I_O = 20\mu\text{A}$	2.0			0.5		V
			4.5			1.35		
			6.0			1.8		
$V_{OH}$	High-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9		1.9	V
			$I_{OH} = -20\mu\text{A}$	4.5	4.4		4.4	
			$I_{OH} = -20\mu\text{A}$	6.0	5.9		5.9	
			$I_{OH} = -4.0\text{mA}$	4.5	4.18		4.13	
			$I_{OH} = -5.2\text{mA}$	6.0	5.68		5.63	
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0		0.1	0.1	V
			$I_{OL} = 20\mu\text{A}$	4.5		0.1	0.1	
			$I_{OL} = 20\mu\text{A}$	6.0		0.1	0.1	
			$I_{OL} = 4.0\text{mA}$	4.5		0.26	0.33	
			$I_{OL} = 5.2\text{mA}$	6.0		0.26	0.33	
$I_{IH}$	High-level input current	$V_I = 6\text{V}$	6.0			0.1	1.0	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0\text{V}$	6.0			-0.1	-1.0	
$I_{CC}$	Quiescent supply current	$V_I = V_{CC}, \text{GND}, I_O = 0\mu\text{A}$	6.0			1.0	10.0	$\mu\text{A}$

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE

**SWITCHING CHARACTERISTICS** ( $V_{CC} = 5V$ ,  $T_a = 25^\circ C$ )

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{TLH}$	Low-level to high-level and high-level to low-level output transition time	C <sub>L</sub> = 15pF (Note 2)			10	ns
$t_{THL}$	Low-level to high-level and high-level to low-level output transition time				10	ns
$t_{PLH}$	Low-level to high-level and high-level to low-level output propagation time	C <sub>L</sub> = 15pF (Note 2)			20	ns
$t_{PHL}$	Low-level to high-level and high-level to low-level output propagation time				20	ns

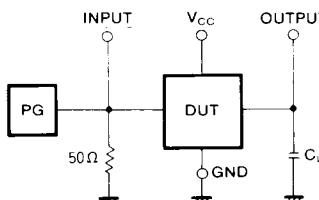
**SWITCHING CHARACTERISTICS** ( $V_{CC} = 2\sim 6V$ ,  $T_a = -40\sim +85^\circ C$ )

Symbol	Parameter	Test conditions	Limits					Unit
			25°C		-40~+85°C			
V <sub>CC</sub> (V)	Min	Typ	Max	Min	Max			
$t_{TLH}$	Low-level to high-level and high-level to low-level output transition time	C <sub>L</sub> = 50pF (Note 2)	2.0		75	95		ns
			4.5		15	19		
			6.0		13	16		
			2.0		75	95		
			4.5		15	19		
			6.0		13	16		
$t_{THL}$	Low-level to high-level and high-level to low-level output transition time	C <sub>L</sub> = 50pF (Note 2)	2.0		120	151		ns
			4.5		24	30		
			6.0		20	26		
			2.0		120	151		
			4.5		24	30		
			6.0		20	26		
C <sub>I</sub>	Input capacitance				10	10	pF	
C <sub>PD</sub>	Power dissipation capacitance (Note 1)				38		pF	

Note 1 : C<sub>PD</sub> is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)  
The power dissipated during operation under no-load conditions is calculated using the following formula:

$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$$

Note 2 : Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): t<sub>r</sub> = 6ns, t<sub>f</sub> = 6ns
- (2) The capacitance C<sub>L</sub> includes stray wiring capacitance and the probe input capacitance.

**TIMING DIAGRAM**

