

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4510B **MSI** **BCD up/down counter**

Product specification
File under Integrated Circuits, IC04

January 1995

BCD up/down counter

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DESCRIPTION

The HEF4510B is an edge-triggered synchronous up/down BCD counter with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input (CE), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P₀ to P₃), four parallel outputs (O₀ to O₃), an active LOW terminal count output (TC), and an overriding asynchronous master reset input (MR).

Information on P₀ to P₃ is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW to HIGH transition of CP if CE is LOW. UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, TC is LOW when O₀ and O₃ are HIGH and CE is LOW. When counting down, TC is LOW when O₀ to O₃ and CE are LOW. A HIGH on MR resets the counter (O₀ to O₃ = LOW) independent of all other input conditions.

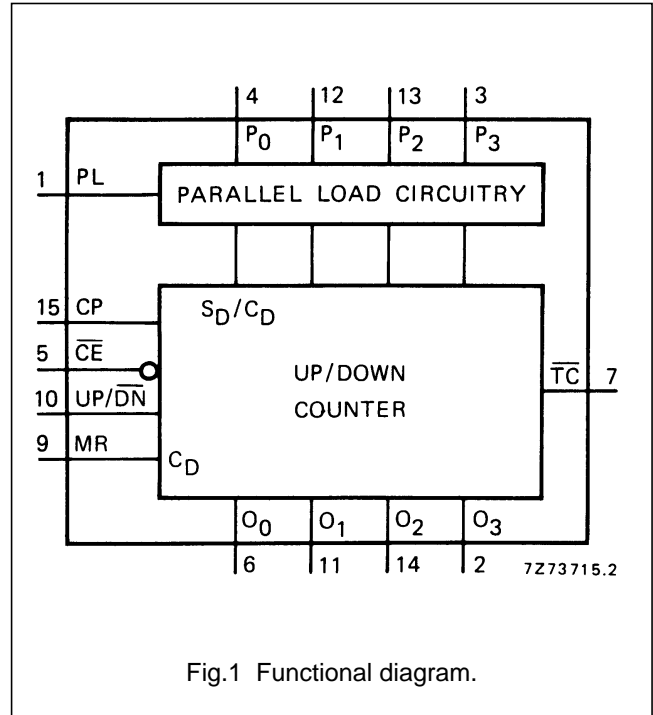


Fig.1 Functional diagram.

- HEF4510BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4510BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4510BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- PL parallel load input (active HIGH)
- P₀ to P₃ parallel inputs
- CE count enable input (active LOW)
- CP clock pulse input (LOW to HIGH, edge triggered)
- UP/DN up/down count control input
- MR master reset input
- TC terminal count output (active LOW)
- O₀ to O₃ parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

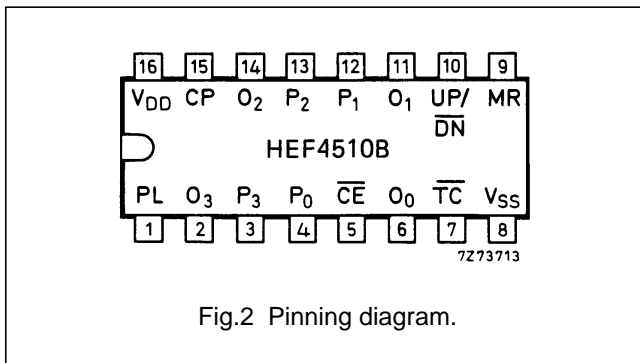


Fig.2 Pinning diagram.

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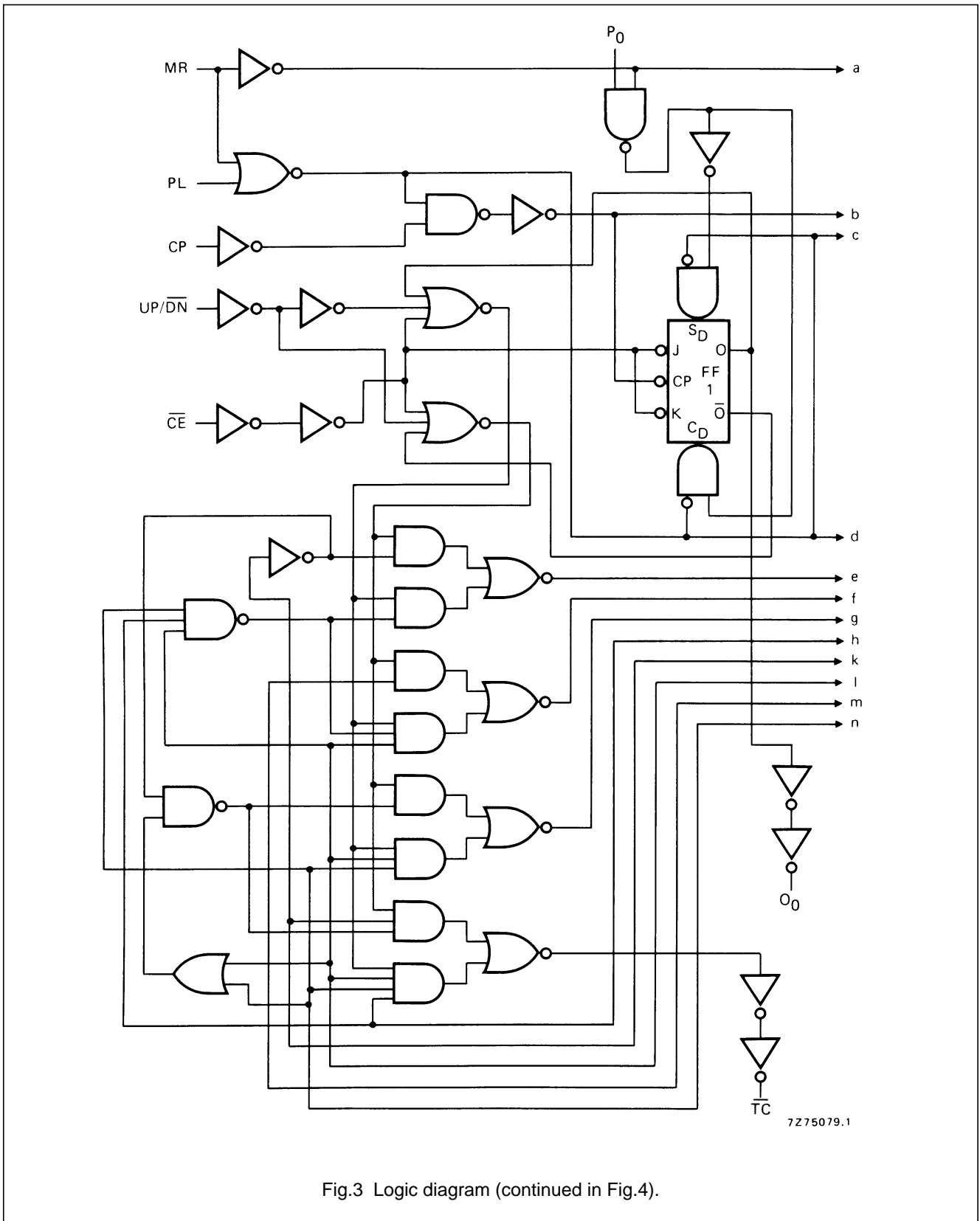
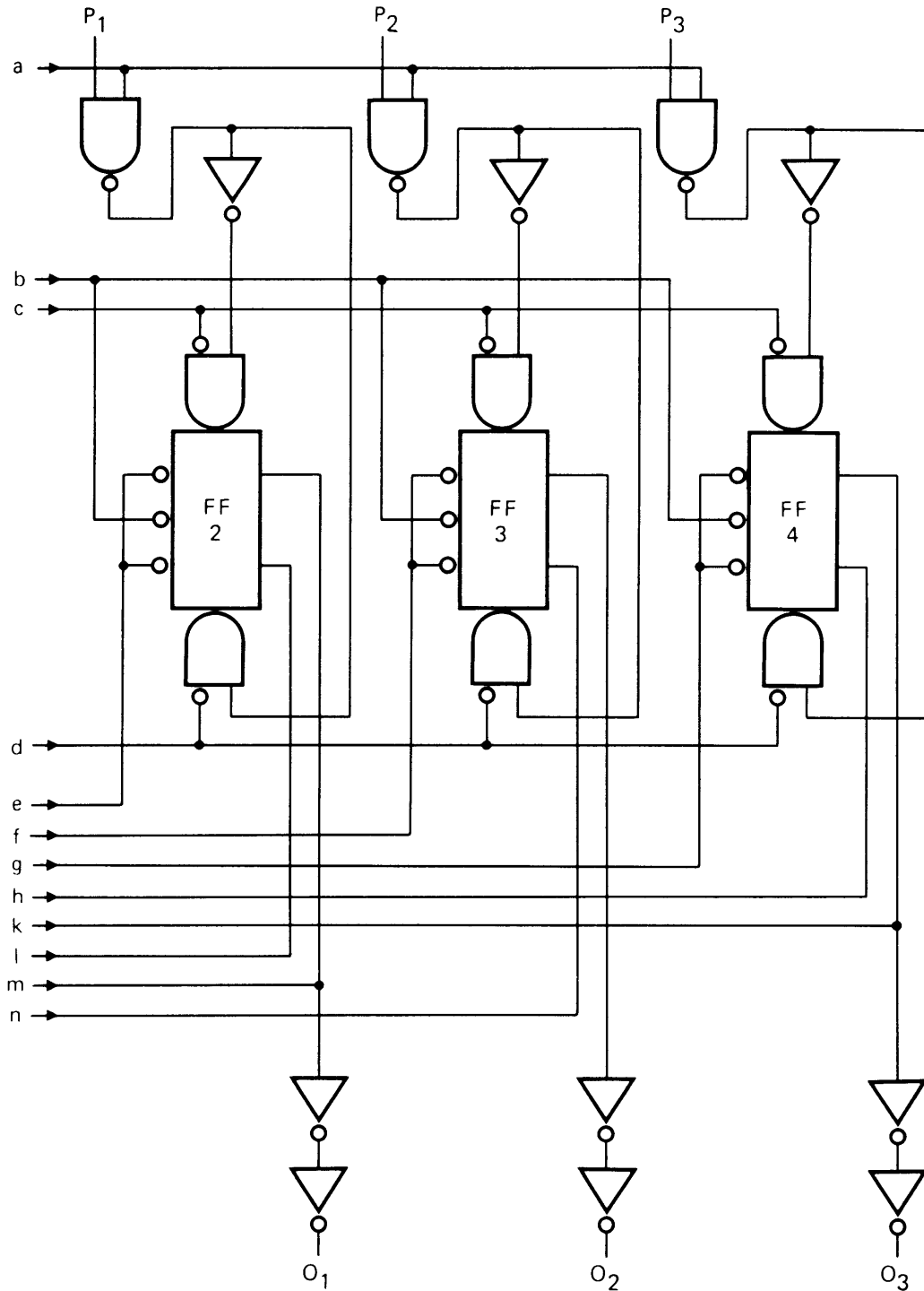


Fig.3 Logic diagram (continued in Fig.4).

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Fig.4 Logic diagram (continued from Fig.3).

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FUNCTION TABLE

MR	PL	UP/DN	CE	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↗	count down
L	L	H	L	↖	count up
H	X	X	X	X	reset

Notes

- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition

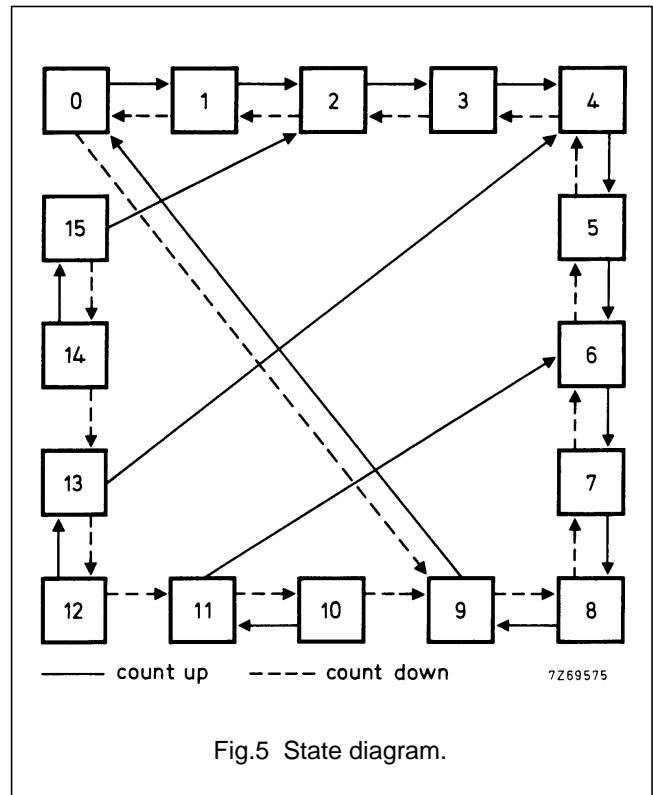


Fig.5 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{CE} \cdot \{ (UP/DN) \cdot O_0 \cdot O_3 + (\overline{UP/DN}) \cdot \overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	1000 f _i + ∑ (f _o C _L) × V _{DD} ² 4500 f _i + ∑ (f _o C _L) × V _{DD} ² 11 200 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays							
CP \rightarrow O _n	5			145	290	ns	118 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C _L
	15			45	90	ns	37 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		155	310	ns	128 ns + (0,55 ns/pF) C _L
	10			65	130	ns	54 ns + (0,23 ns/pF) C _L
	15			45	90	ns	37 ns + (0,16 ns/pF) C _L
CP \rightarrow \overline{TC}	5			260	525	ns	233 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		105	210	ns	94 ns + (0,23 ns/pF) C _L
	15			75	150	ns	67 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		180	360	ns	153 ns + (0,55 ns/pF) C _L
	10			75	150	ns	64 ns + (0,23 ns/pF) C _L
	15			55	115	ns	47 ns + (0,16 ns/pF) C _L
PL \rightarrow O _n	5			125	255	ns	98 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C _L
	15			40	85	ns	32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		170	340	ns	143 ns + (0,55 ns/pF) C _L
	10			70	140	ns	59 ns + (0,23 ns/pF) C _L
	15			50	105	ns	42 ns + (0,16 ns/pF) C _L
PL \rightarrow \overline{TC}	5			250	500	ns	223 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		110	220	ns	99 ns + (0,23 ns/pF) C _L
	15			80	160	ns	72 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		250	500	ns	223 ns + (0,55 ns/pF) C _L
	10			110	220	ns	99 ns + (0,23 ns/pF) C _L
	15			80	160	ns	72 ns + (0,16 ns/pF) C _L
$\overline{CE} \rightarrow \overline{TC}$	5			165	330	ns	138 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		65	135	ns	54 ns + (0,23 ns/pF) C _L
	15			50	100	ns	42 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		145	290	ns	118 ns + (0,55 ns/pF) C _L
	10			60	125	ns	49 ns + (0,23 ns/pF) C _L
	15			45	95	ns	37 ns + (0,16 ns/pF) C _L
MR \rightarrow O _n , \overline{TC}	5			205	405	ns	178 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C _L
	15			45	85	ns	37 ns + (0,16 ns/pF) C _L
MR \rightarrow \overline{TC}	5			225	450	ns	198 ns + (0,55 ns/pF) C _L
LOW to HIGH	10	t _{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C _L
	15			50	100	ns	42 ns + (0,16 ns/pF) C _L

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	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Output transition times HIGH to LOW	5	t_{THL}		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA					
Minimum clock pulse width; LOW	5	t _{WCPL}	95	45	ns	see also waveforms Figs 6 and 7					
	10		35	20	ns						
	15		25	15	ns						
Minimum PL pulse width; HIGH	5	t _{WPLH}	105	55	ns						
	10		45	25	ns						
	15		35	15	ns						
Minimum MR pulse width; HIGH	5	t _{WMRH}	120	60	ns						
	10		50	25	ns						
	15		40	20	ns						
Recovery time for MR	5	t _{RMR}	130	65	ns						
	10		45	20	ns						
	15		30	15	ns						
Recovery time for PL	5	t _{RPL}	150	75	ns						
	10		50	25	ns						
	15		30	15	ns						
Set-up times	5	t _{su}	100	50	ns						
							P _n → PL	10	50	25	ns
	5	t _{su}	250	125	ns						
							UP/DN → CP	10	100	50	ns
	5	t _{su}	120	60	ns						
							CE → PL	10	40	20	ns
5	t _{hold}	10	-40	ns							
					P _n → PL		10	5	-20	ns	
											15
5	t _{hold}	35	-90	ns							
					UP/DN → CP	10	15	-35	ns		
										15	15
5	t _{hold}	20	-40	ns							
					CE → CP	10	5	-15	ns		
										15	5
5	f _{max}	5	10	MHz							
					Maximum clock pulse frequency	10	12	24	MHz		
										15	17

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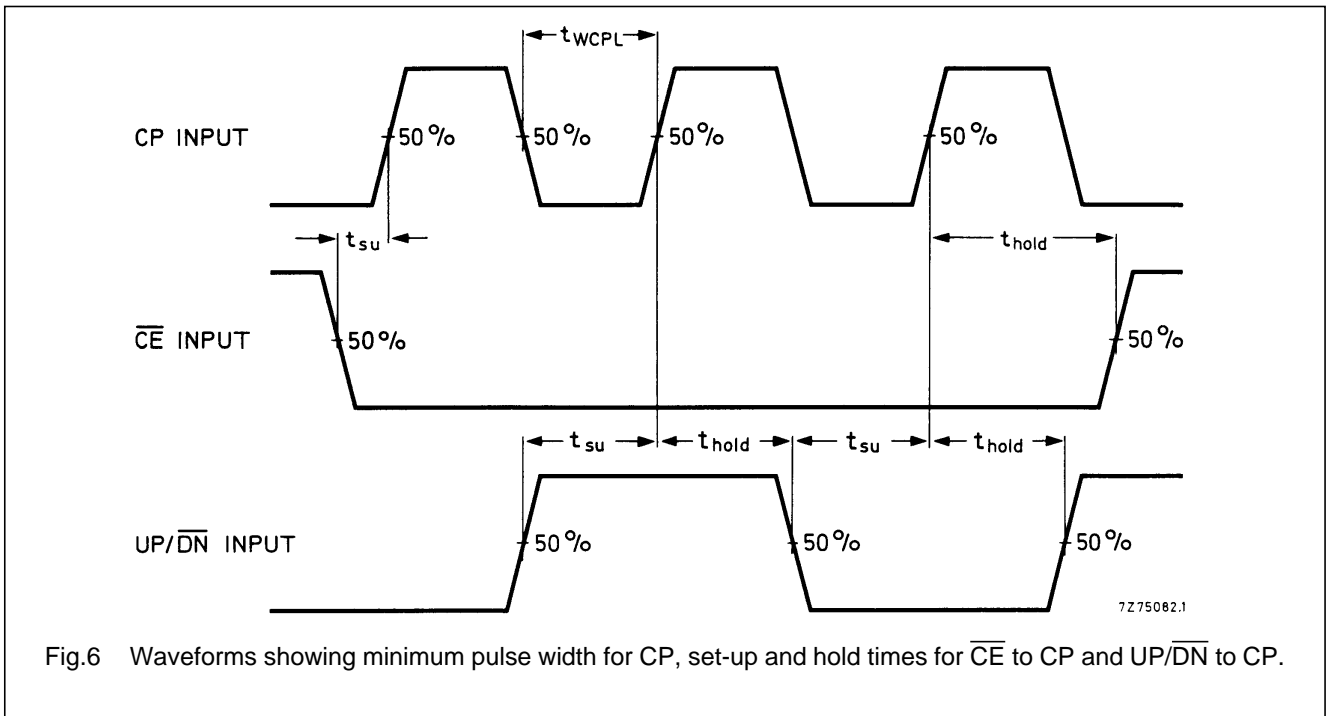


Fig.6 Waveforms showing minimum pulse width for CP, set-up and hold times for \overline{CE} to CP and UP/ \overline{DN} to CP.

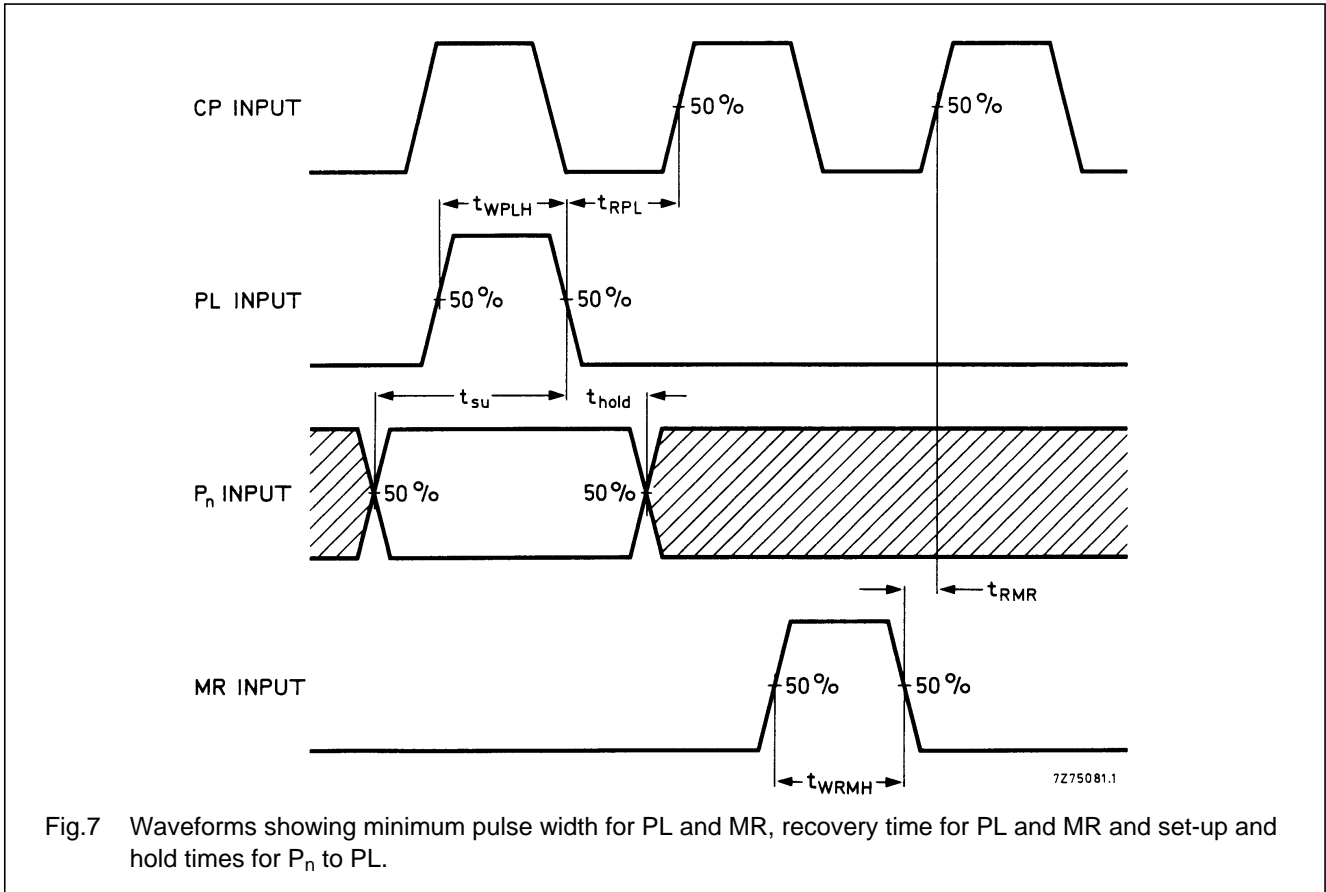
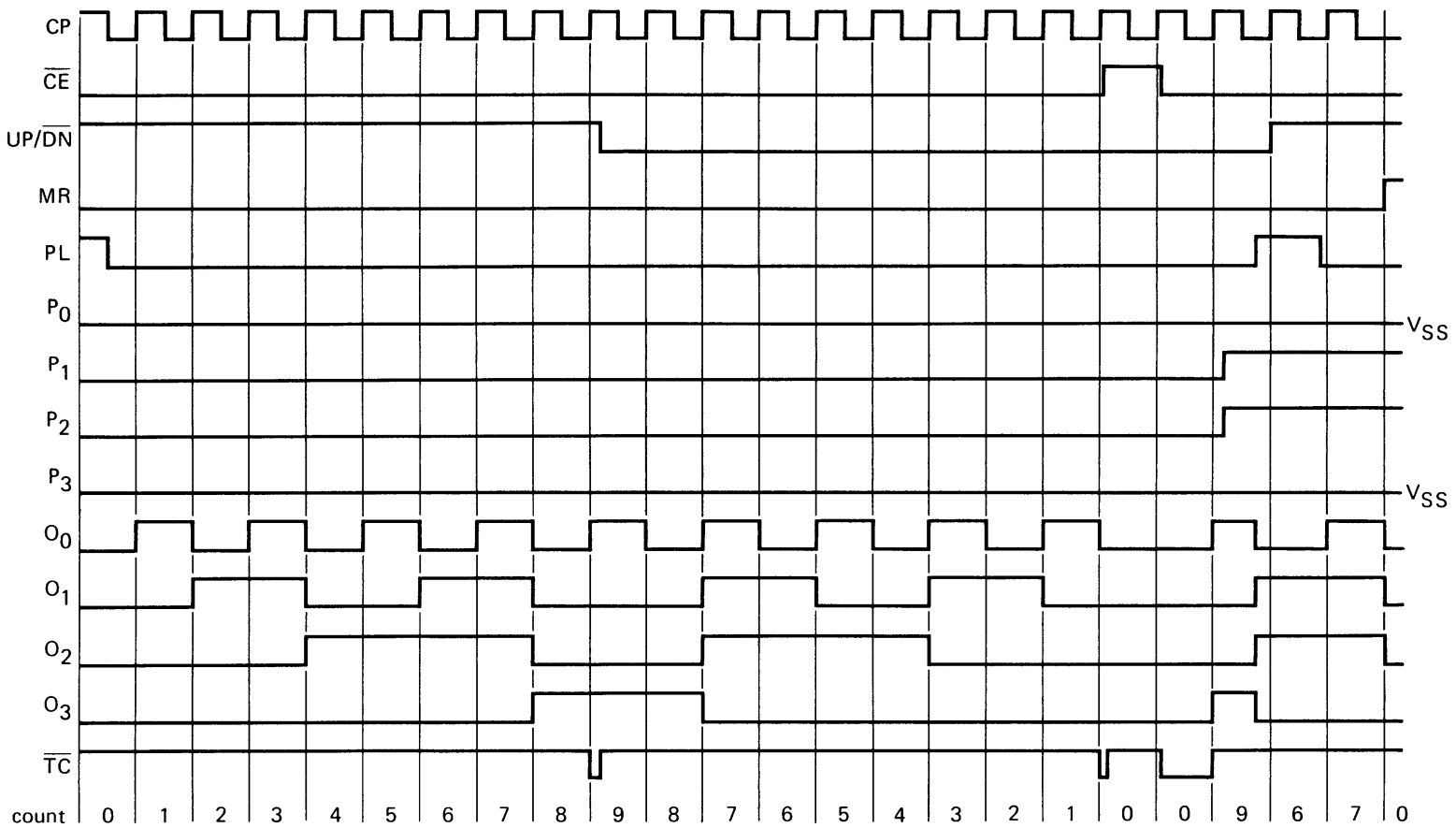


Fig.7 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

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Fig.8 Timing diagram.